

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR
 NP32N055HDE, NP32N055IDE, NP32N055SDE

SWITCHING
 N-CHANNEL POWER MOSFET

DESCRIPTION

These products are N-channel MOS Field Effect Transistor designed for high current switching applications.

FEATURES

- Channel temperature 175 degree rated
- Super low on-state resistance
 $R_{DS(on)1} = 24 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 16 \text{ A)}$
 $R_{DS(on)2} = 29 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5.0 \text{ V, } I_D = 16 \text{ A)}$
- Low C_{iss} : $C_{iss} = 1300 \text{ pF TYP.}$

★ ORDERING INFORMATION

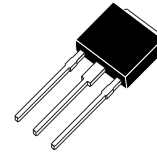
| PART NUMBER | PACKAGE |
|-----------------------------|-------------------------|
| NP32N055HDE | TO-251 (JEITA) / MP-3 |
| NP32N055IDE ^{Note} | TO-252 (JEITA) / MP-3Z |
| NP32N055SDE | TO-252 (JEDEC) / MP-3ZK |

Note Not for new design.

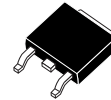
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

| | | | |
|---|-----------------------|---------------|----|
| Drain to Source Voltage (V _{GS} = 0 V) | V _{DSS} | 55 | V |
| Gate to Source Voltage (V _{DS} = 0 V) | V _{GSS} | ±20 | V |
| Drain Current (DC) (T _C = 25°C) | I _{D(DC)} | ±32 | A |
| Drain Current (pulse) ^{Note1} | I _{D(pulse)} | ±100 | A |
| Total Power Dissipation (T _C = 25°C) | P _{T1} | 66 | W |
| Total Power Dissipation (T _A = 25°C) | P _{T2} | 1.2 | W |
| Channel Temperature | T _{ch} | 175 | °C |
| Storage Temperature | T _{stg} | -55 to +175 | °C |
| Single Avalanche Current ^{Note2} | I _{AS} | 28 / 21 / 8 | A |
| Single Avalanche Energy ^{Note2} | E _{AS} | 7.8 / 44 / 64 | mJ |

(TO-251)



(TO-252)



- Notes 1. $PW \leq 10 \mu s$, Duty Cycle $\leq 1\%$
 2. Starting T_{ch} = 25°C, R_G = 25 Ω, V_{GS} = 20 → 0 V

THERMAL RESISTANCE

| | | | |
|---------------------------------------|-----------------------|------|------|
| Channel to Case Thermal Resistance | R _{th(ch-C)} | 2.27 | °C/W |
| Channel to Ambient Thermal Resistance | R _{th(ch-A)} | 125 | °C/W |

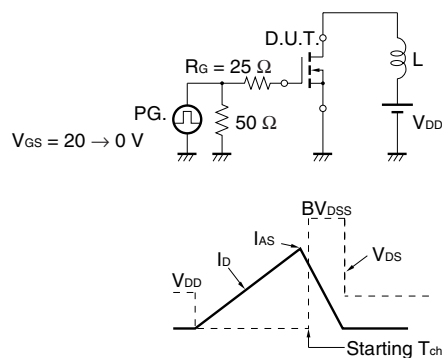
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ELECTRICAL CHARACTERISTICS (T_A = 25°C)

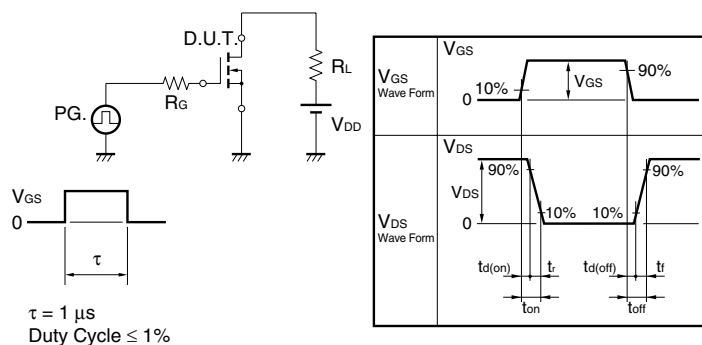
| CHARACTERISTICS | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|----------------------|---|------|------|------|------|
| Zero Gate Voltage Drain Current | I _{DSS} | V _{DS} = 55 V, V _{GS} = 0 V | | | 10 | μA |
| Gate Leakage Current | I _{GSS} | V _{GS} = ±20 V, V _{DS} = 0 V | | | ±100 | nA |
| Gate to Source Threshold Voltage | V _{GS(th)} | V _{DS} = V _{GS} , I _D = 250 μA | 1.5 | 2 | 2.5 | V |
| Forward Transfer Admittance Note | y _{fs} | V _{DS} = 10 V, I _D = 16 A | 8 | 16 | | S |
| Drain to Source On-state Resistance Note | R _{DS(on)1} | V _{GS} = 10 V, I _D = 16 A | | 19 | 24 | mΩ |
| | R _{DS(on)2} | V _{GS} = 5.0 V, I _D = 16 A | | 22 | 29 | mΩ |
| | R _{DS(on)3} | V _{GS} = 4.5 V, I _D = 16 A | | 24 | 33 | mΩ |
| Input Capacitance | C _{iss} | V _{DS} = 25 V | | 1300 | 2000 | pF |
| Output Capacitance | C _{oss} | V _{GS} = 0 V | | 180 | 270 | pF |
| Reverse Transfer Capacitance | C _{rss} | f = 1 MHz | | 90 | 160 | pF |
| Turn-on Delay Time | t _{d(on)} | V _{DD} = 28 V, I _D = 16 A | | 14 | 31 | ns |
| Rise Time | t _r | V _{GS} = 10 V | | 8 | 20 | ns |
| Turn-off Delay Time | t _{d(off)} | R _G = 1 Ω | | 40 | 81 | ns |
| Fall Time | t _f | | | 7.4 | 19 | ns |
| Total Gate Charge | Q _{G1} | V _{DD} = 44 V, V _{GS} = 10 V, I _D = 32 A | | 27 | 41 | nC |
| | Q _{G2} | V _{DD} = 44 V | | 15 | 23 | nC |
| Gate to Source Charge | Q _{GS} | V _{GS} = 5.0 V | | 5 | | nC |
| Gate to Drain Charge | Q _{GD} | I _D = 32 A | | 9 | | nC |
| Body Diode Forward Voltage Note | V _{F(S-D)} | I _F = 32 A, V _{GS} = 0 V | | 1.0 | | V |
| Reverse Recovery Time | t _{rr} | I _F = 32 A, V _{GS} = 0 V | | 41 | | ns |
| Reverse Recovery Charge | Q _{rr} | di/dt = 100 A/μs | | 58 | | nC |

Note Pulsed

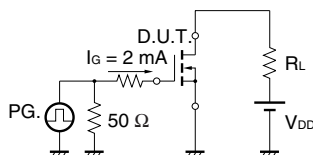
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25°C)

Figure1. DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

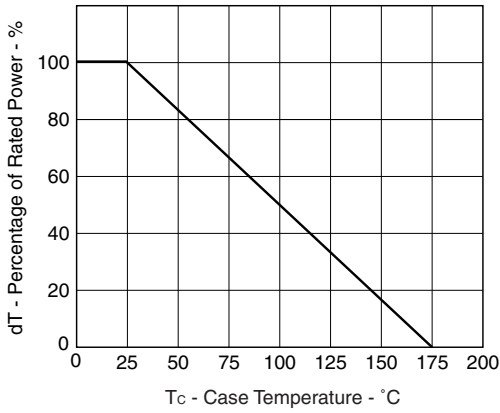


Figure2. TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

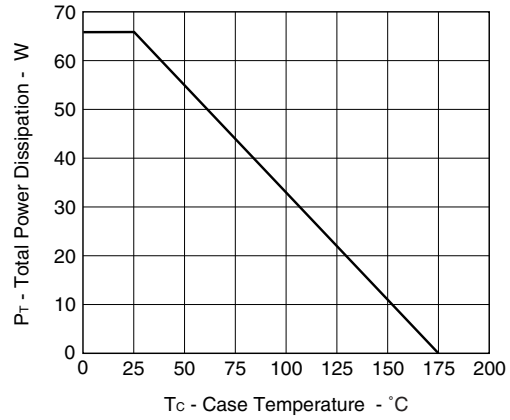


Figure3. FORWARD BIAS SAFE OPERATING AREA

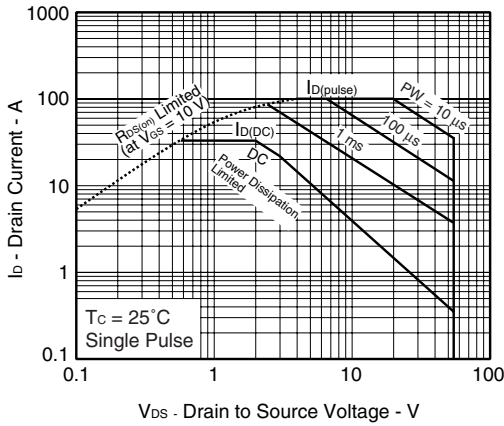


Figure4. SINGLE AVALANCHE ENERGY DERATING FACTOR

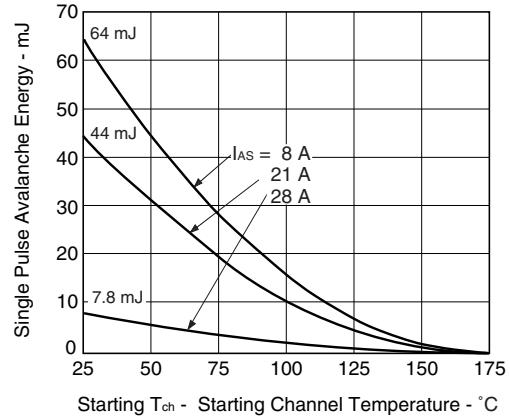


Figure5. TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH

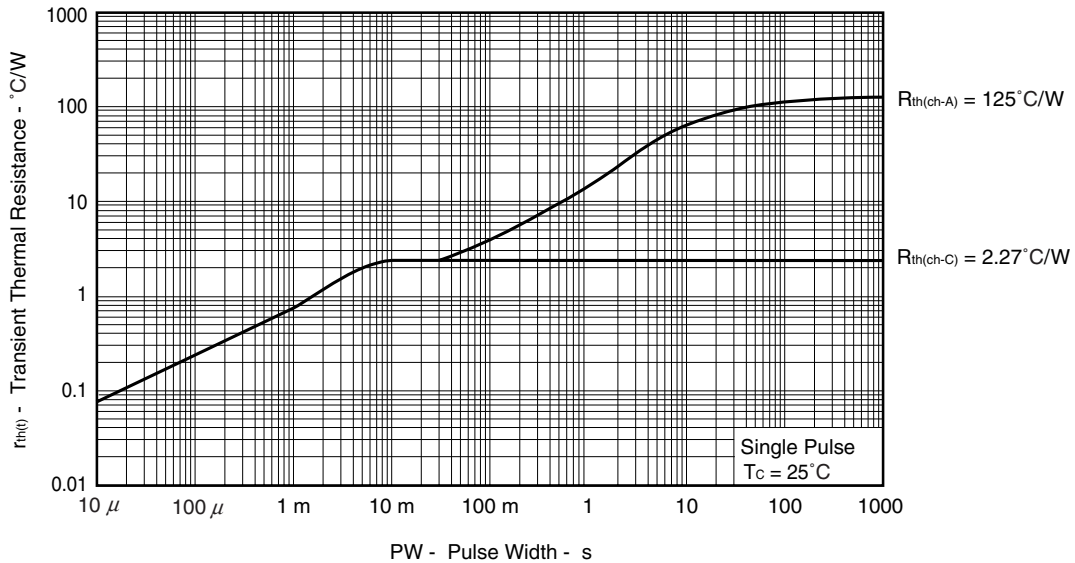


Figure6. FORWARD TRANSFER CHARACTERISTICS

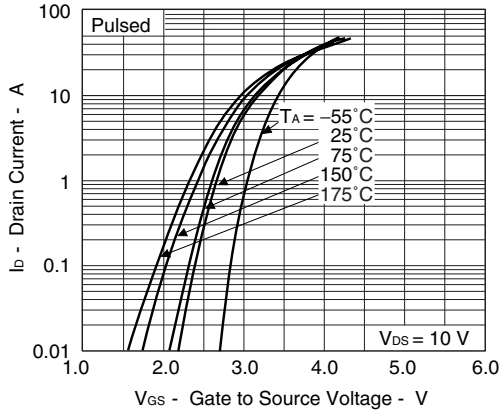


Figure7. DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE

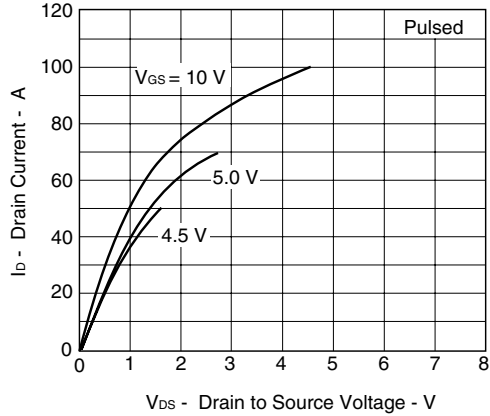


Figure8. FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT

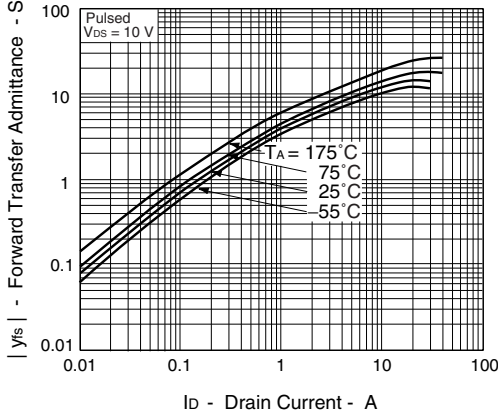


Figure9. DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

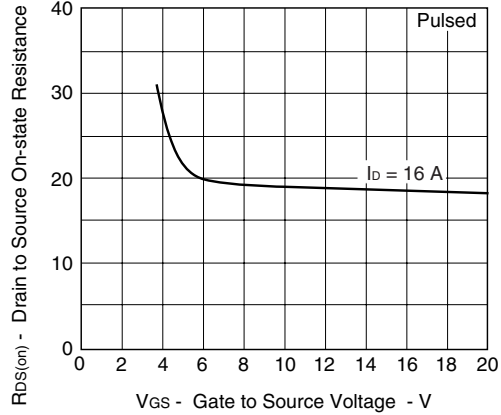


Figure10. DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT

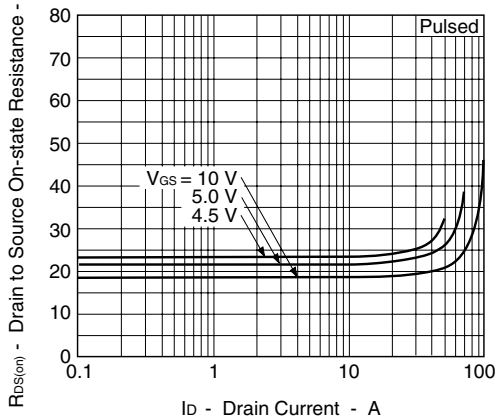


Figure11. GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE

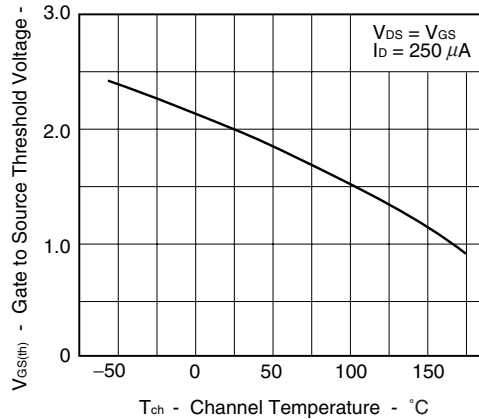


Figure12. DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE

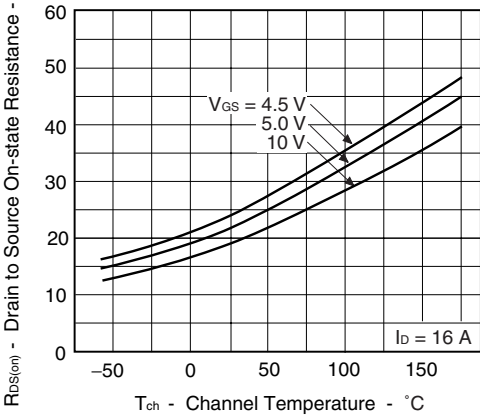


Figure13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

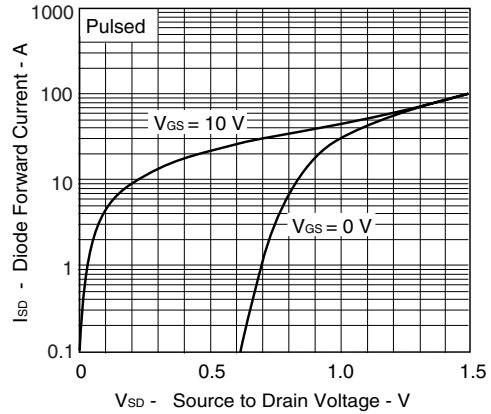


Figure14. CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

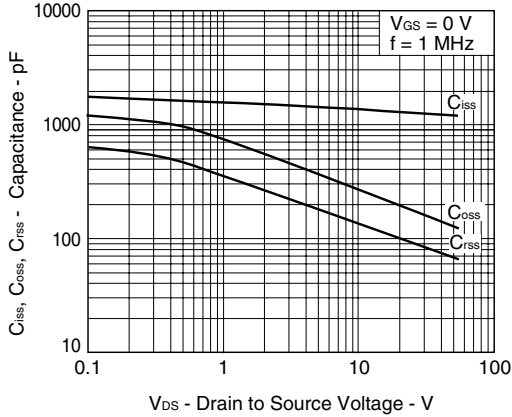


Figure15. SWITCHING CHARACTERISTICS

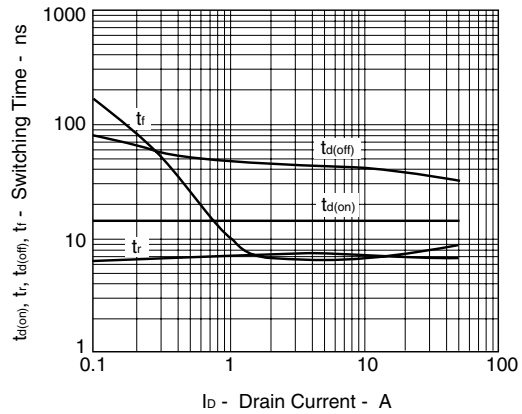


Figure16. REVERSE RECOVERY TIME vs. DRAIN CURRENT

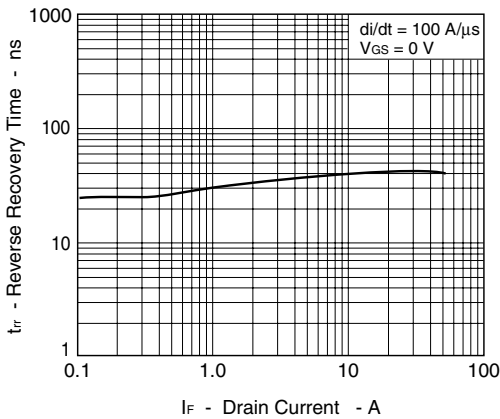
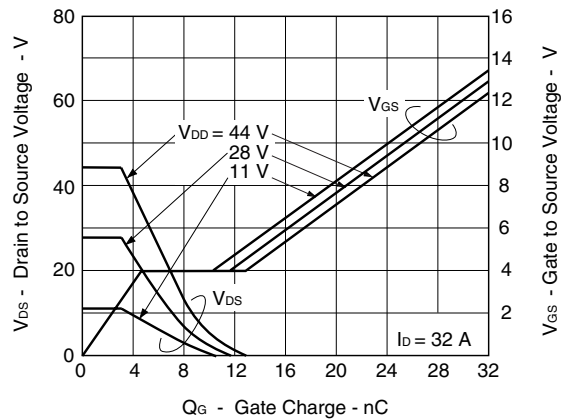
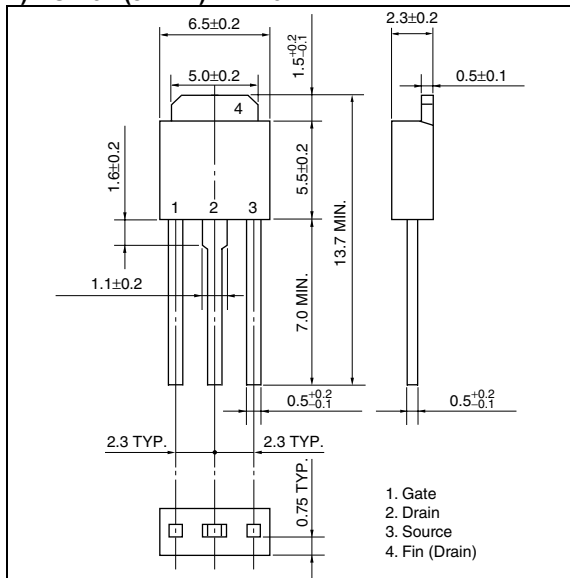


Figure17. DYNAMIC INPUT/OUTPUT CHARACTERISTICS

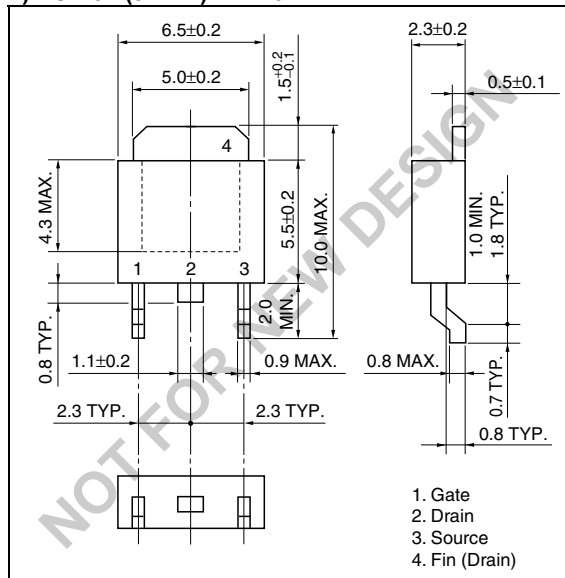


★ PACKAGE DRAWINGS (Unit: mm)

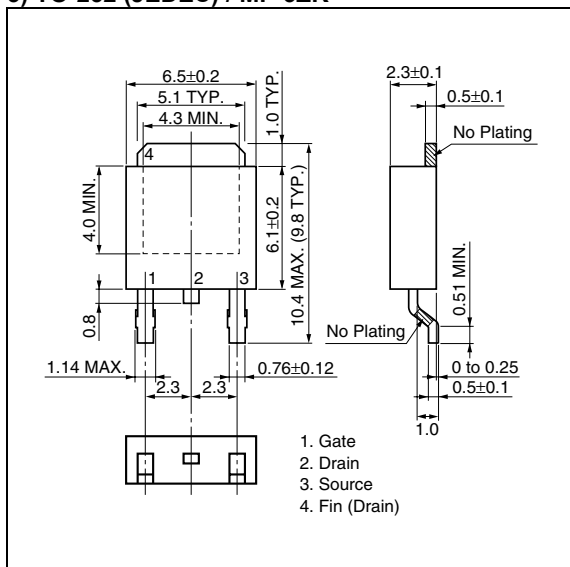
1) TO-251 (JEITA) / MP-3



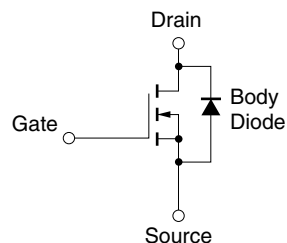
2) TO-252 (JEITA) / MP-3Z



3) TO-252 (JEDEC) / MP-3ZK



EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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