

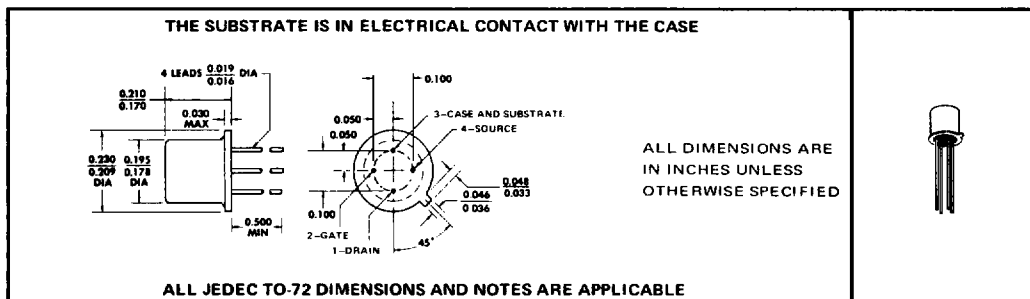
**TYPE 3N160**  
**P-CHANNEL ENHANCEMENT-TYPE**  
**INSULATED-GATE FIELD-EFFECT TRANSISTOR**  
 BULLETIN NO. DL-S 7011149, MARCH 1970

**ENHANCEMENT-TYPE† MOS SILICON TRANSISTOR**

For Applications Requiring Very High Input Impedance, Such as  
 Series and Shunt Choppers, Multiplexers, and Commutators

- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Diode-Protected Version Available . . . 3N161

**\*mechanical data**



**handling precautions**

Curve-tracer testing and static-charge buildup are common causes of damage to insulated-gate devices. Permanent damage may result if either gate-voltage rating is exceeded even for extremely short time periods. Each transistor is protected during shipment by a gate-shorting device, which should be removed only during testing and after permanent mounting of the transistor. Personnel and equipment, including soldering irons, should be grounded.

**\*absolute maximum ratings at 25°C free-air temperature (unless otherwise noted)**

Drain-Gate Voltage . . . . .	-25 V
Drain-Source Voltage . . . . .	-25 V
Forward Gate-Source Voltage . . . . .	-25 V
Reverse Gate-Source Voltage . . . . .	25 V
Continuous Drain Current . . . . .	-125 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 1) . . . . .	360 mW
Continuous Device Dissipation at (or below) 25°C Case Temperature (See Note 2) . . . . .	1.8 W
Storage Temperature Range . . . . .	-65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds . . . . .	300°C

NOTES: 1. Derate linearly to 175°C free-air temperature at the rate of 2.4 mW/°C.  
 2. Derate linearly to 175°C case temperature at the rate of 12 mW/°C.

†JEDEC registered data. This data sheet contains all applicable registered data in effect at the time of publication.

Enhancement-mode operation entails the use of a forward gate-source voltage to increase drain current from  $I_{DSS}$ , the drain current at  $V_{GS} = 0$ , as opposed to depletion-mode operation wherein a reverse gate-source voltage is used to decrease drain current. An enhancement-type transistor is in the "off" state at  $V_{GS} = 0$  and hence will not operate normally in the depletion mode.

USES CHIP MP92

# TYPE 3N160

## P-CHANNEL ENHANCEMENT-TYPE INSULATED-GATE FIELD-EFFECT TRANSISTOR

\*electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
$I_{GSSF}$	Forward Gate-Terminal Current	$V_{GS} = -25\text{ V}, V_{DS} = 0$		-10	pA
		$V_{GS} = -25\text{ V}, V_{DS} = 0$	$T_A = 100^\circ\text{C}$	-50	pA
$I_{GSSR}$	Reverse Gate-Terminal Current	$V_{GS} = 25\text{ V}, V_{DS} = 0$		10	pA
$I_{DSS}$	Zero-Gate-Voltage Drain Current	$V_{DS} = -15\text{ V}, V_{GS} = 0$		-10	nA
		$V_{DS} = -25\text{ V}, V_{GS} = 0$		-10	$\mu\text{A}$
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{DS} = -15\text{ V}, I_D = -10\ \mu\text{A}$	-1.5	-5	V
$V_{GS}$	Gate-Source Voltage	$V_{DS} = -15\text{ V}, I_D = -8\text{ mA}$	-4.5	-8	V
$I_{D(on)}$	On-State Drain Current	$V_{DS} = -15\text{ V}, V_{GS} = -15\text{ V}$ , See Note 3	-40	-120	mA
$ y_{fs} $	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = -15\text{ V}, I_D = -8\text{ mA}$	3.5	6.5	mmho
$ y_{os} $	Small-Signal Common-Source Output Admittance			0.25	mmho
$C_{iss}$	Common-Source Short-Circuit Input Capacitance		10	pF	
$C_{rss}$	Common-Source Short-Circuit Reverse Transfer Capacitance		4	pF	

NOTE 3: These parameters must be measured using pulse techniques.  $t_p \approx 100\text{ ms}$ , duty cycle  $\leq 10\%$ .

\*JEDEC registered data

†All measurements are made with the third lead (case and substrate) connected to the fourth lead (source).

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### THERMAL INFORMATION

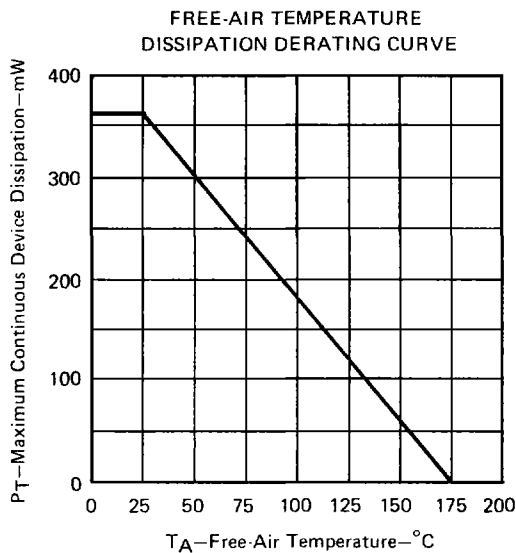


FIGURE 1

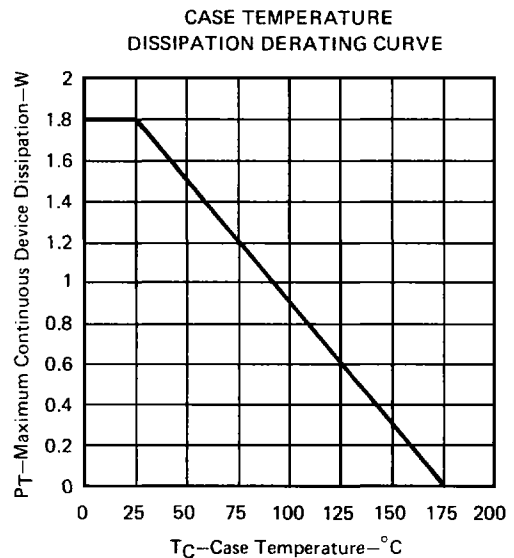


FIGURE 2