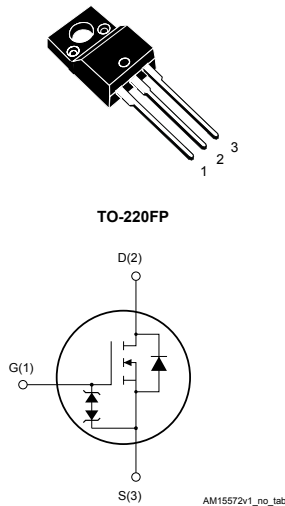


N-channel 950 V, 3 Ω typ., 4 A MDmesh K3 Power MOSFET in a TO-220FP package



Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STF5N95K3	950 V	3.5 Ω	4 A

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

Applications

- Switching applications

Description

This MDmesh K3 Power MOSFET is the result of improvements applied to STMicroelectronics' MDmesh technology, combined with a new optimized vertical structure. This device boasts an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering it suitable for the most demanding applications.

Product status link

[STF5N95K3](#)

Product summary

Order code	STF5N95K3
Marking	5N95K3
Package	TO-220FP
Packing	Tube

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{GS}	Gate-source voltage	±30	V
I _D ⁽¹⁾	Drain current (continuous) at T _C = 25 °C	4	A
	Drain current (continuous) at T _C = 100 °C	3	
I _{DM} ⁽²⁾	Drain current (pulsed)	16	A
P _{TOT}	Total power dissipation at T _C = 25 °C	25	W
I _{AR}	Avalanche current, repetitive or non-repetitive (pulse width limited by T _J max)	4	A
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	100	mJ
dv/dt ⁽³⁾	Peak diode recovery voltage slope	5	V/ns
V _{ISO}	Insulation withstand voltage (RMS) from all three leads to external heat sink (t = 1 s, T _C = 25 °C)	2.5	kV
T _{stg}	Storage temperature range	-55 to 150	°C
T _J	Operating junction temperature range		°C

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 4 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DS} (\text{peak}) \leq V_{(BR)DSS}$.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJA}	Thermal resistance, junction-to-ambient	62.5	°C/W
R _{thJC}	Thermal resistance, junction-to-case	5	°C/W

2 Electrical characteristics

$T_C = 25\text{ °C}$ unless otherwise specified.

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0\text{ V}$	950			V
I_{DSS}	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 950\text{ V}$, $T_C = 125\text{ °C}$ ⁽¹⁾			50	
I_{GSS}	Gate body leakage current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 100\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2\text{ A}$		3	3.5	Ω

1. Specified by design, not tested in production.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0\text{ V}$	-	460	-	pF
C_{oss}	Output capacitance		-	38	-	pF
C_{riss}	Reverse transfer capacitance		-	1	-	pF
$C_{o(tr)}$ ⁽¹⁾	Equivalent output capacitance time related	$V_{GS} = 0\text{ V}$, $V_{DS} = 0\text{ to }760\text{ V}$	-	970	-	pF
$C_{o(er)}$ ⁽²⁾	Equivalent output capacitance energy related		-	15	-	pF
R_g	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_D = 0\text{ A}$	-	5.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 760\text{ V}$, $I_D = 4\text{ A}$, $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 15. Test circuit for gate charge behavior)	-	19	-	nC
Q_{gs}	Gate-source charge		-	4.7	-	nC
Q_{gd}	Gate-drain charge		-	12	-	nC

1. $C_{o(tr)}$ is a constant capacitance value that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

2. $C_{o(er)}$ is a constant capacitance value that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS} .

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 475\text{ V}$, $I_D = 2\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 14. Test circuit for resistive load switching times and Figure 19. Switching time waveform)	-	17	-	ns
t_r	Rise time		-	7	-	ns
$t_{d(off)}$	Turn-off delay time		-	32	-	ns
t_f	Fall time		-	18	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		16	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4\text{ A}, V_{GS} = 0\text{ V}$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V}$	-	410		ns
Q_{rr}	Reverse recovery charge	(see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	3.5		μC
I_{RRM}	Reverse recovery current		-	17		A
t_{rr}	Reverse recovery time	$I_{SD} = 4\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, V_{DD} = 60\text{ V},$	-	516		ns
Q_{rr}	Reverse recovery charge	$T_J = 150\text{ }^\circ\text{C}$ (see Figure 16. Test circuit for inductive load switching and diode recovery times)	-	4.1		μC
I_{RRM}	Reverse recovery current		-	16		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

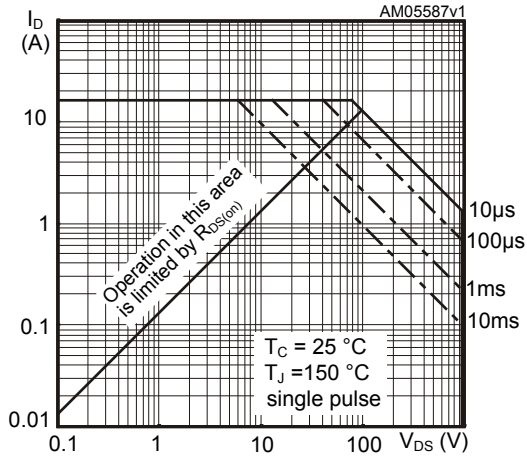


Figure 2. Normalized transient thermal impedance

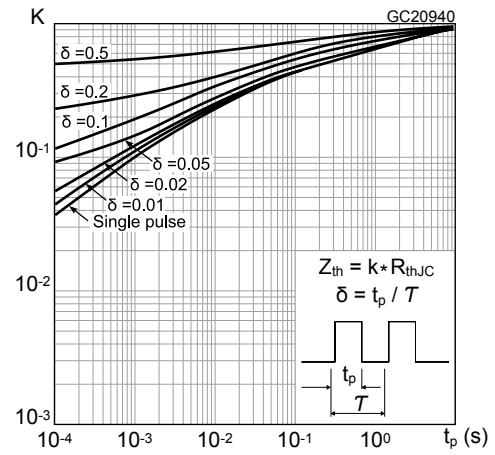


Figure 3. Typical output characteristics

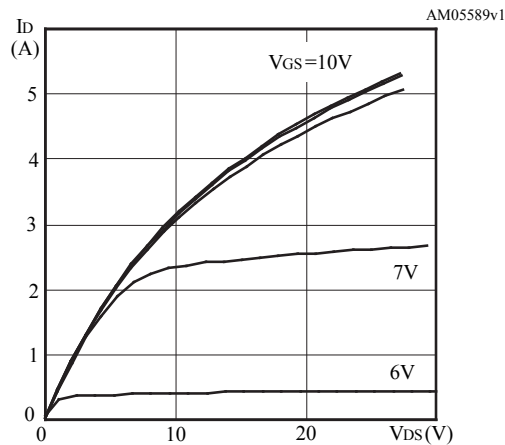


Figure 4. Typical transfer characteristics

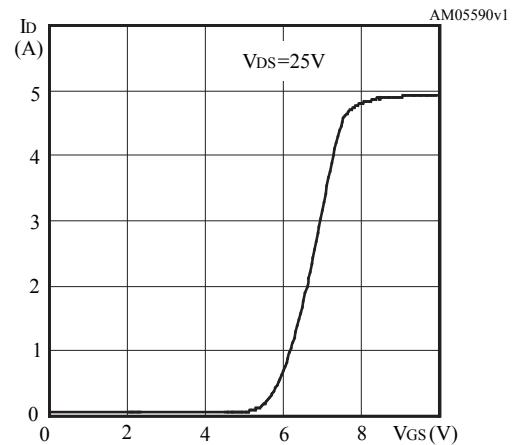


Figure 5. Typical gate charge characteristics

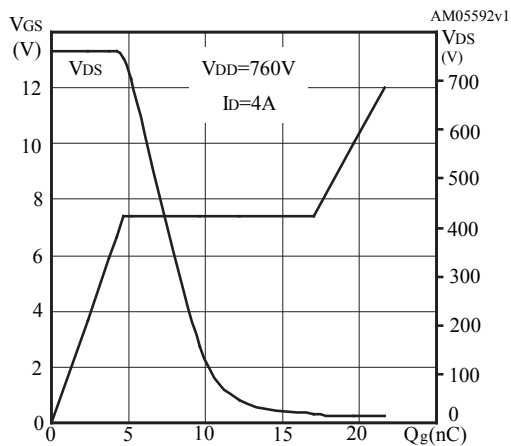


Figure 6. Typical drain-source on-resistance

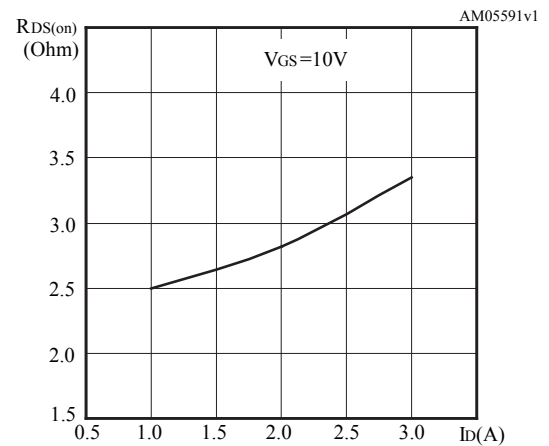


Figure 7. Typical capacitance characteristics

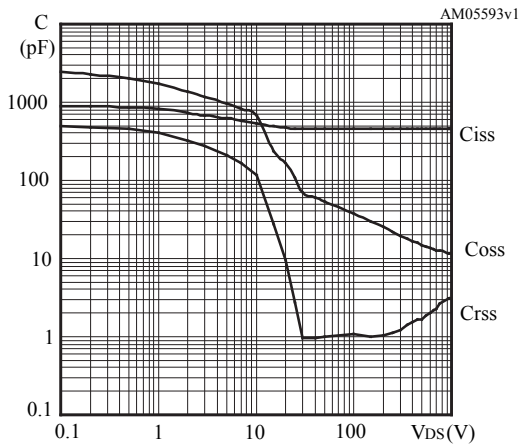


Figure 8. Typical output capacitance stored energy

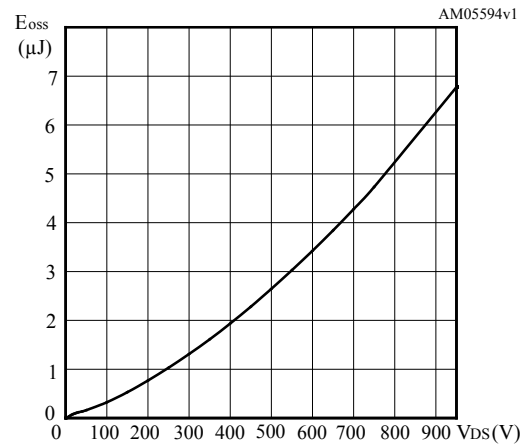


Figure 9. Normalized gate threshold vs temperature

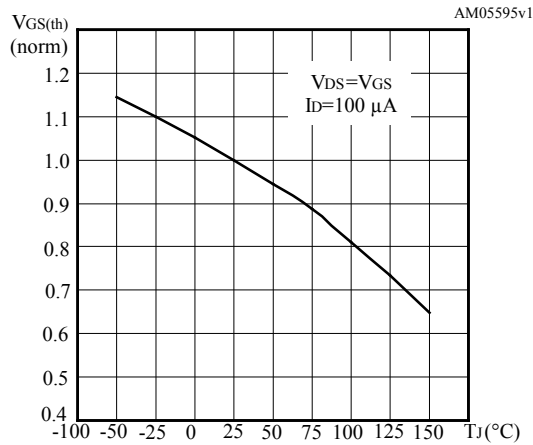


Figure 10. Normalized on-resistance vs temperature

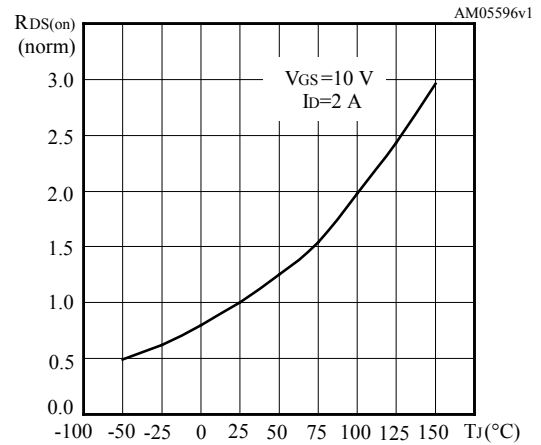


Figure 11. Normalized breakdown voltage vs temperature

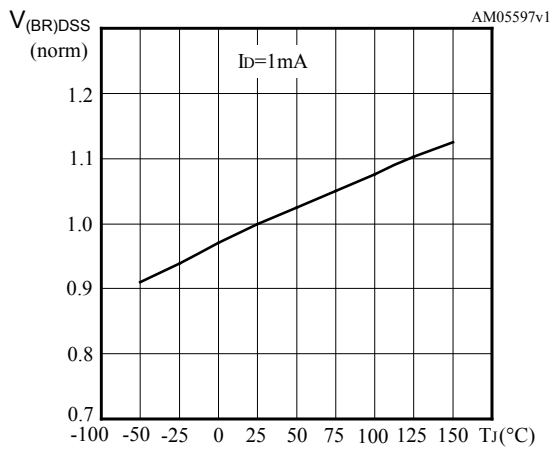


Figure 12. Typical reverse diode forward characteristics

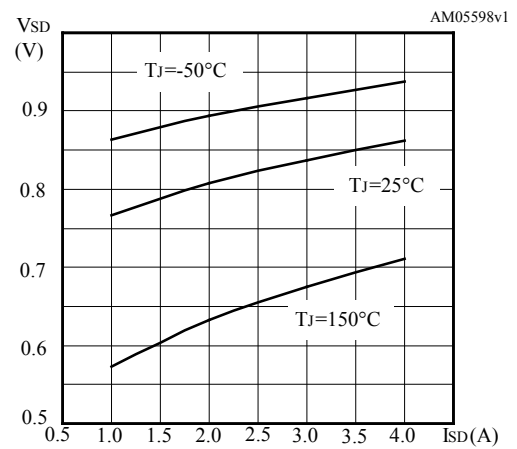
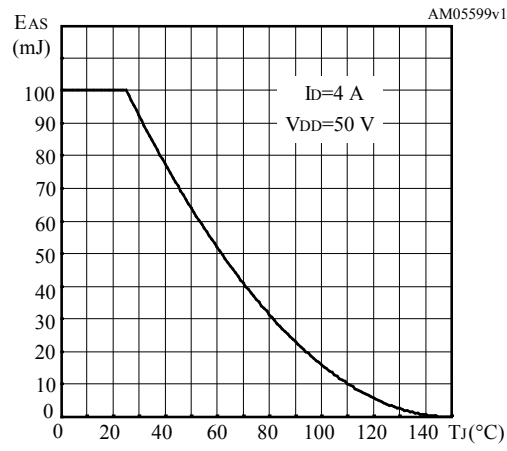
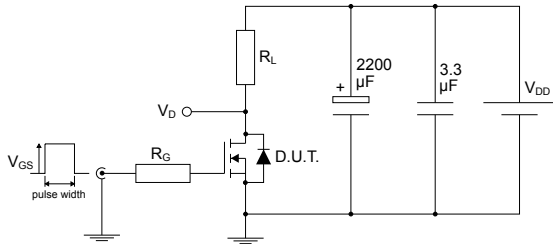


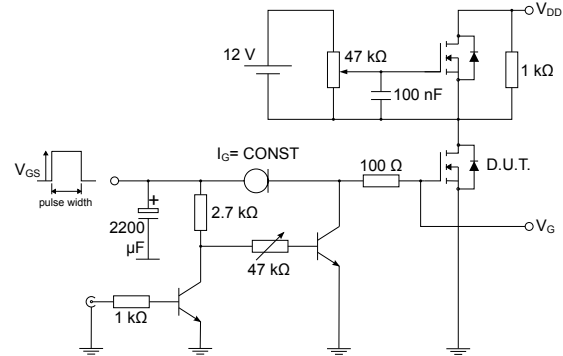
Figure 13. Maximum avalanche energy vs temperature



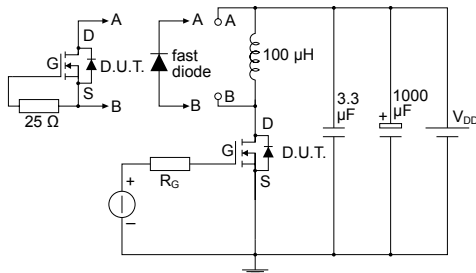
3 Test circuits

Figure 14. Test circuit for resistive load switching times


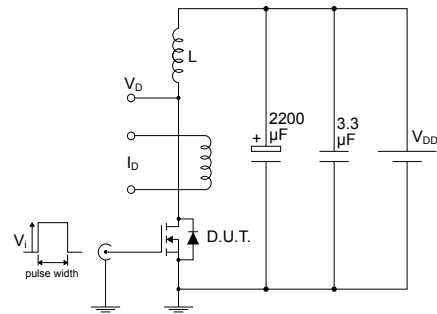
AM01468v1

Figure 15. Test circuit for gate charge behavior


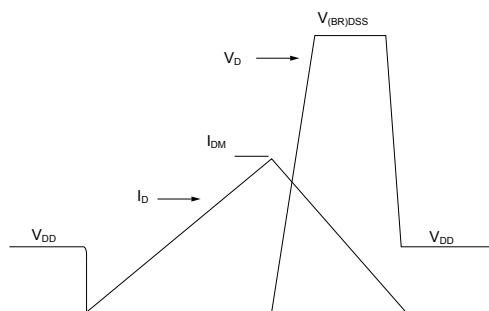
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Figure 16. Test circuit for inductive load switching and diode recovery times


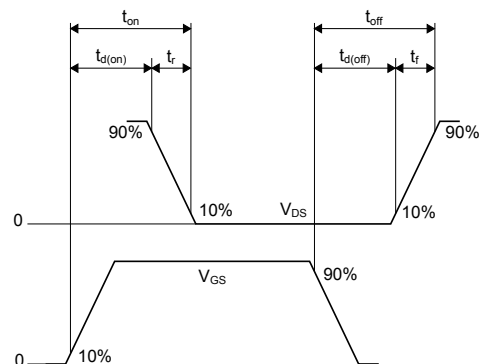
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Figure 17. Unclamped inductive load test circuit


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Figure 18. Unclamped inductive waveform


AM01472v1

Figure 19. Switching time waveform


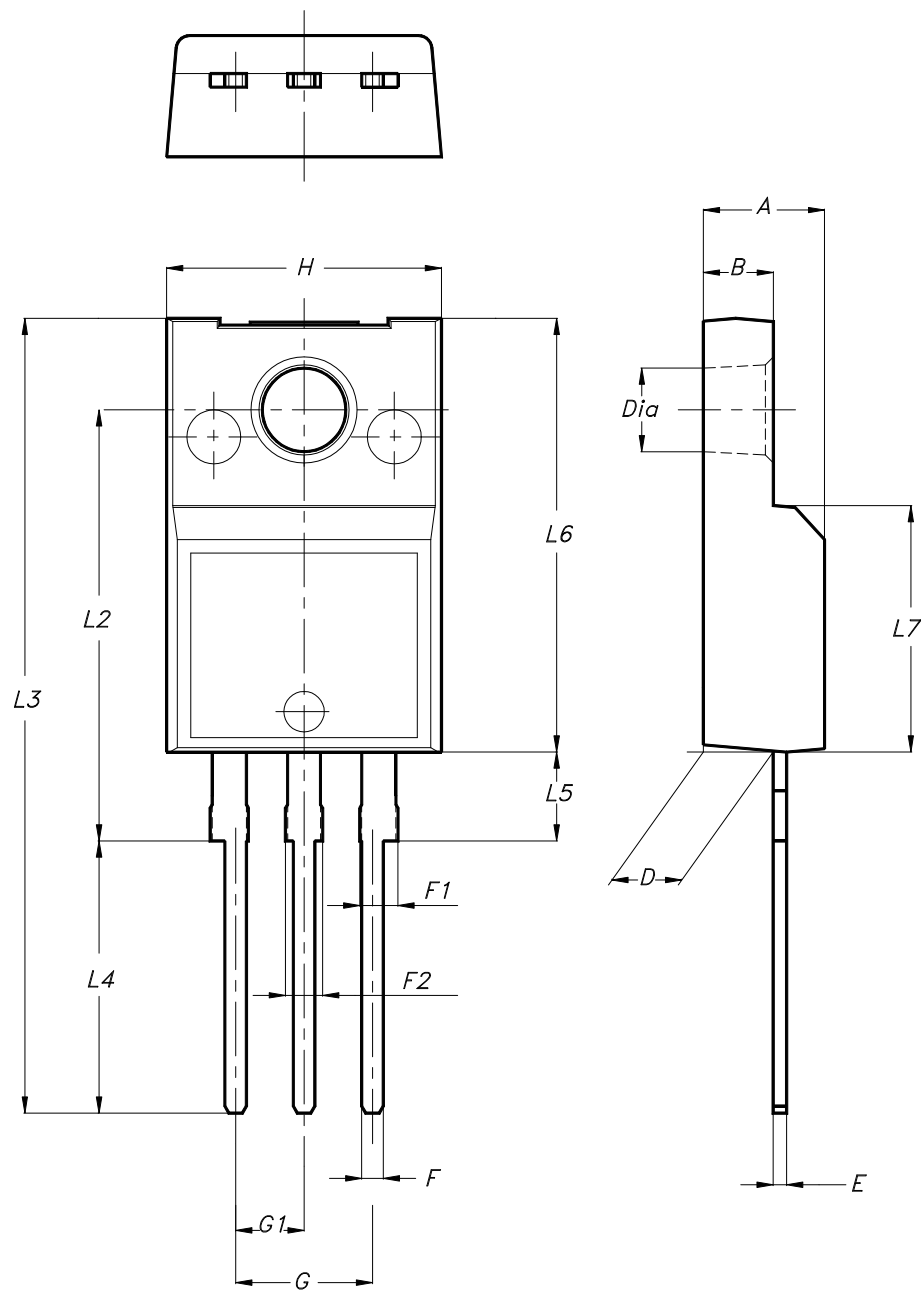
AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 TO-220FP type B package information

Figure 20. TO-220FP type B package outline



7012510_B_rev.14

Table 7. TO-220FP type B package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
E	0.45		0.70
F	0.75		1.00
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.20
G1	2.40		2.70
H	10.00		10.40
L2		16.00	
L3	28.60		30.60
L4	9.80		10.60
L5	2.90		3.60
L6	15.90		16.40
L7	9.00		9.30
Dia	3.00		3.20

4.2 TO-220FP type C package information

Figure 21. TO-220FP type C package outline

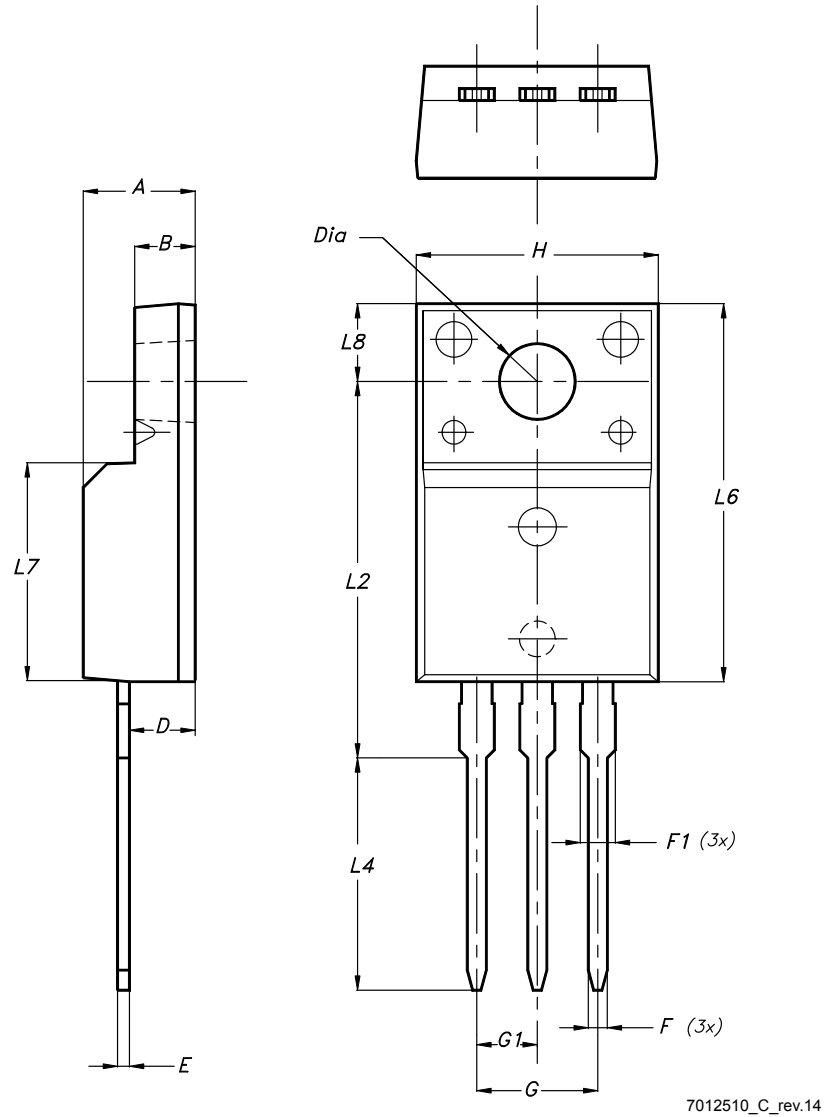


Table 8. TO-220FP type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.50		4.90
B	2.34		2.74
D	2.56		2.96
E	0.45	0.50	0.60
F	0.70		0.90
F1	1.15		1.70
G		5.08	
G1	2.34	2.54	2.74
H	9.96		10.36
L2		15.80	
L4	9.45		10.05
L6	15.67		16.07
L7	8.99		9.39
L8		3.30	
Dia	3.08		3.28

Revision history

Table 9. Document revision history

Date	Version	Changes
02-May-2023	1	First release. Part number previously included in datasheet DS6265

Contents

1	Electrical ratings	2
2	Electrical characteristics	3
2.1	Electrical characteristics (curves)	5
3	Test circuits	8
4	Package information	9
4.1	TO-220FP type B package information	9
4.2	TO-220FP type C package information	11
	Revision history	13

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