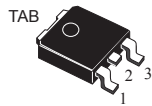
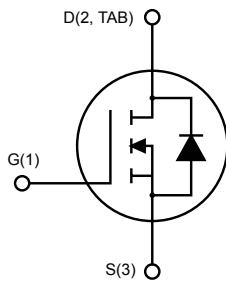


N-channel 60 V, 70 mΩ typ., 12 A, StripFET™ II Power MOSFET in a DPAK package


DPAK


AM01475v1_noZen

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D
STD12NF06LT4	60 V	90 mΩ	12 A

- Exceptional dv/dt capability
- 100% avalanche tested
- Low gate charge

Applications

- Switching applications

Description

This Power MOSFET series has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

Product status link

[STD12NF06LT4](#)

Product summary

Order code	STD12NF06LT4
Marking	D12NF06L
Package	DPAK
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	60	V
V_{GS}	Gate-source voltage	± 16	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^{\circ}\text{C}$	12	A
	Drain current (continuous) at $T_{case} = 100\text{ }^{\circ}\text{C}$	8.5	
$I_{DM}^{(1)}$	Drain current (pulsed)	48	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^{\circ}\text{C}$	30	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$E_{AS}^{(3)}$	Single pulse avalanche energy	100	mJ
T_{stg}	Storage temperature range	-55 to 175	$^{\circ}\text{C}$
T_J	Operating junction temperature range		

1. Pulse width is limited by safe operating area.
2. $I_{SD} \leq 12\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DS} \leq 40\text{ V}$, $T_J \leq T_{JMAX}$
3. Starting $T_J = 25\text{ }^{\circ}\text{C}$, $I_D = 6\text{ A}$, $V_{DD} = 30\text{ V}$

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	5	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	50	

1. When mounted on a 1-inch² FR-4, 2 Oz copper board.

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	60			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 60\text{ V}$			1	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 60\text{ V}$, $T_{\text{case}} = 125\text{ °C}^{(1)}$			10	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 16\text{ V}$			± 100	nA
$V_{\text{GS(th)}}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	1		2	V
$R_{\text{DS(on)}}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 6\text{ A}$		70	90	m Ω
		$V_{\text{GS}} = 5\text{ V}$, $I_{\text{D}} = 6\text{ A}$		80	100	

1. Defined by design, not subject to production test.

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 25\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	350		μF
C_{oss}	Output capacitance		-	75		
C_{riss}	Reverse transfer capacitance		-	30		
Q_{g}	Total gate charge	$V_{\text{DD}} = 48\text{ V}$, $I_{\text{D}} = 12\text{ A}$,	-	7.5	10	nC
Q_{gs}	Gate-source charge	$V_{\text{GS}} = 0\text{ to }5\text{ V}$	-	2.5		
Q_{gd}	Gate-drain charge	(see Figure 13. Test circuit for gate charge behavior)	-	3.0		

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d(on)}}$	Turn-on delay time	$V_{\text{DD}} = 30\text{ V}$, $I_{\text{D}} = 6\text{ A}$, $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 4.5\text{ V}$	-	10	-	ns
t_{r}	Rise time		-	35	-	
$t_{\text{d(off)}}$	Turn-off delay time	(see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	20	-	
t_{f}	Fall time		-	13	-	

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		12	A
$I_{\text{SDM}}^{(1)}$	Source-drain current (pulsed)		-		48	A

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 12\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 12\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 16\text{ V}$, $T_J = 150\text{ }^\circ\text{C}$ (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	50		ns
Q_{rr}	Reverse recovery charge		-	65		nC
I_{RRM}	Reverse recovery current		-	2.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

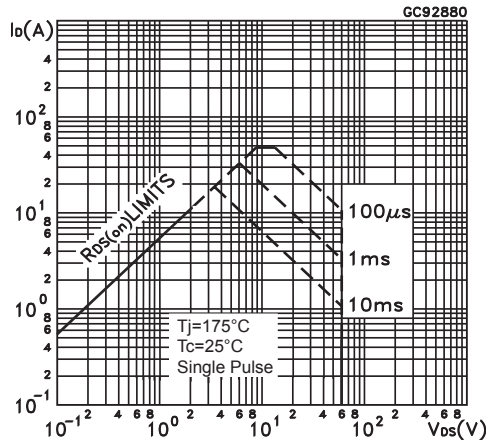


Figure 2. Thermal impedance

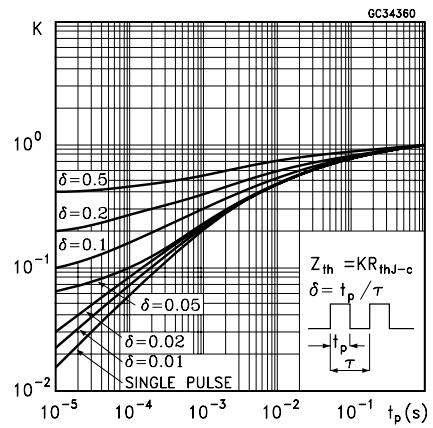


Figure 3. Output characteristics

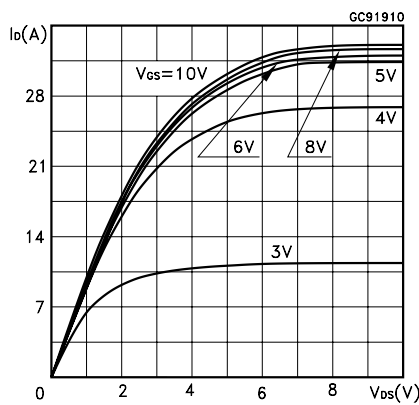


Figure 4. Transfer characteristics

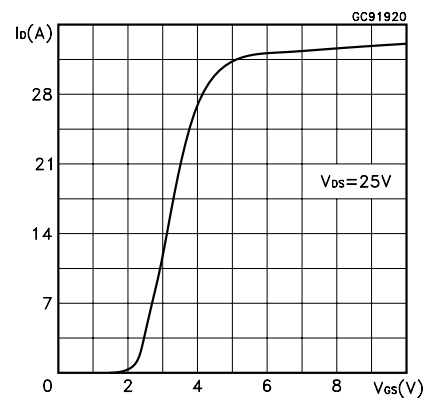


Figure 5. Normalized $V_{(BR)DSS}$ vs temperature

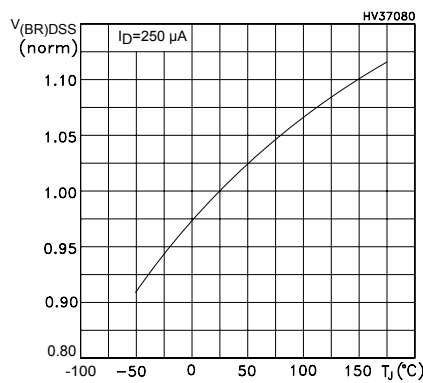


Figure 6. Static drain-source on-resistance

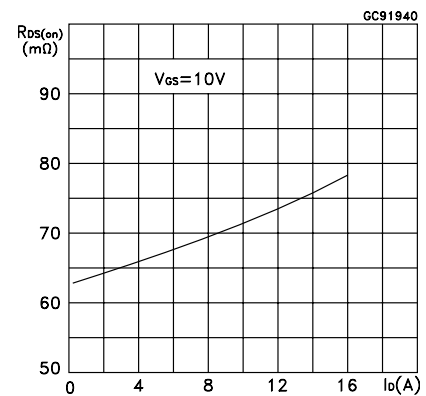


Figure 7. Gate charge vs gate-source voltage

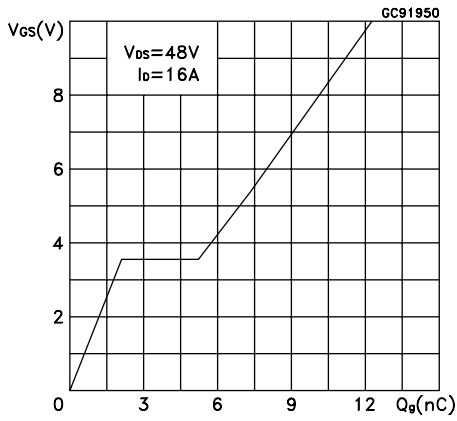


Figure 8. Capacitance variations

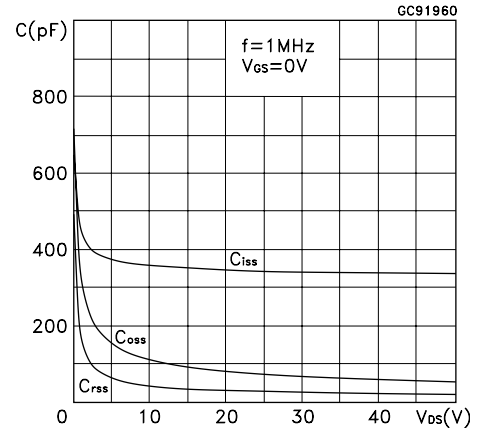


Figure 9. Normalized gate threshold vs temperature

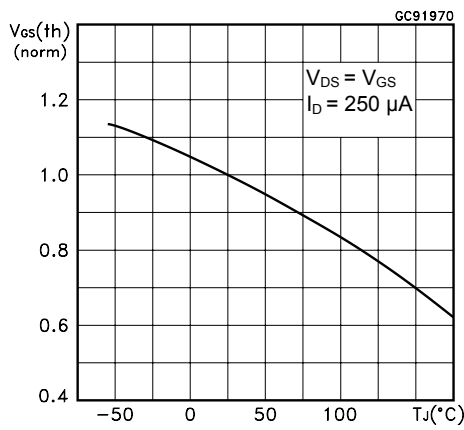


Figure 10. Normalized on-resistance vs temperature

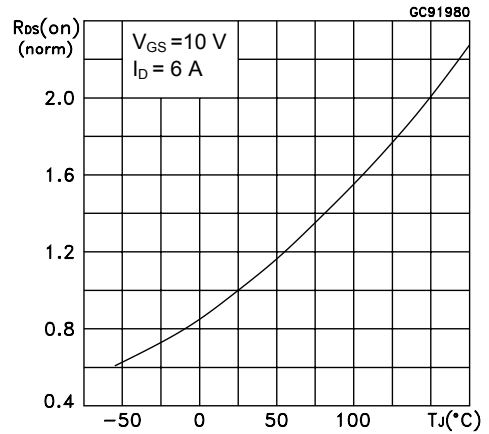
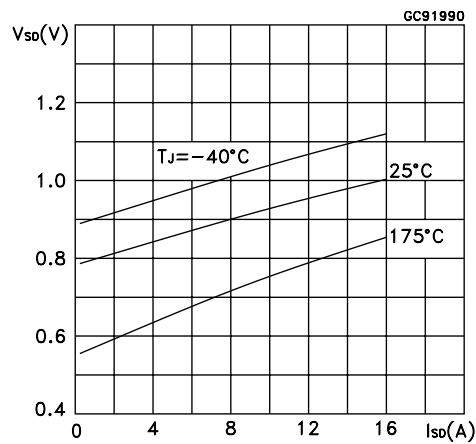
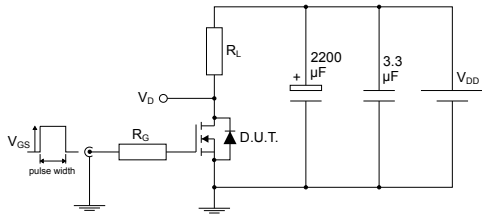


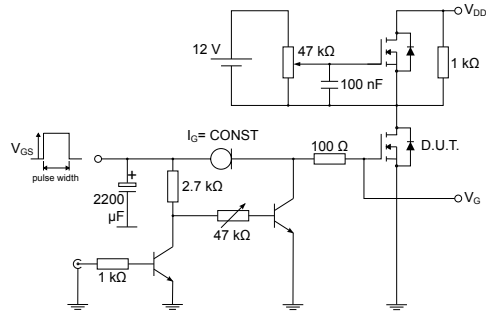
Figure 11. Source-drain diode forward characteristics



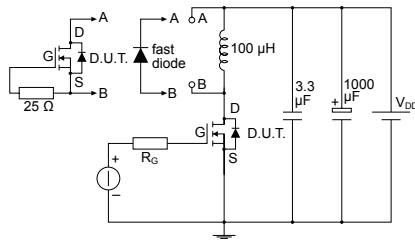
3 Test circuits

Figure 12. Test circuit for resistive load switching times


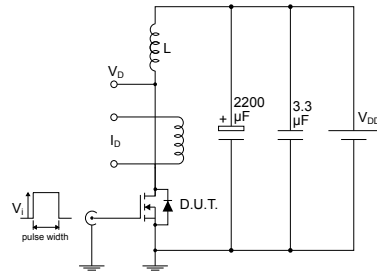
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Figure 13. Test circuit for gate charge behavior


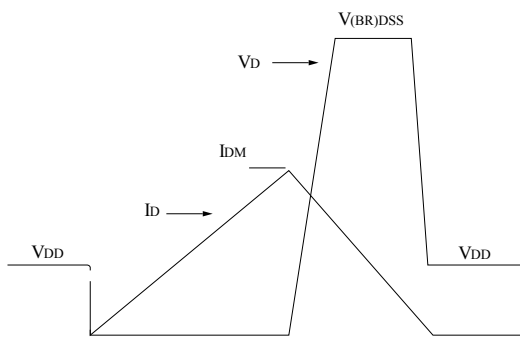
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Figure 14. Test circuit for inductive load switching and diode recovery times


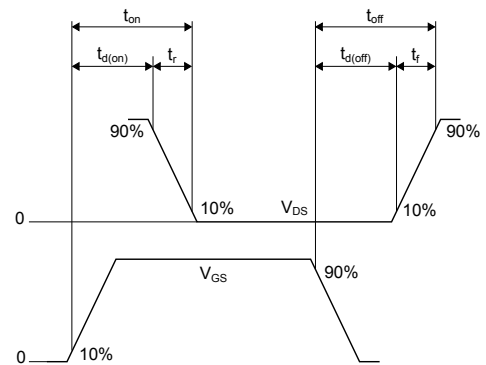
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Figure 15. Unclamped inductive load test circuit


AM01471v1

Figure 16. Unclamped inductive waveform


AM01472v1

Figure 17. Switching time waveform


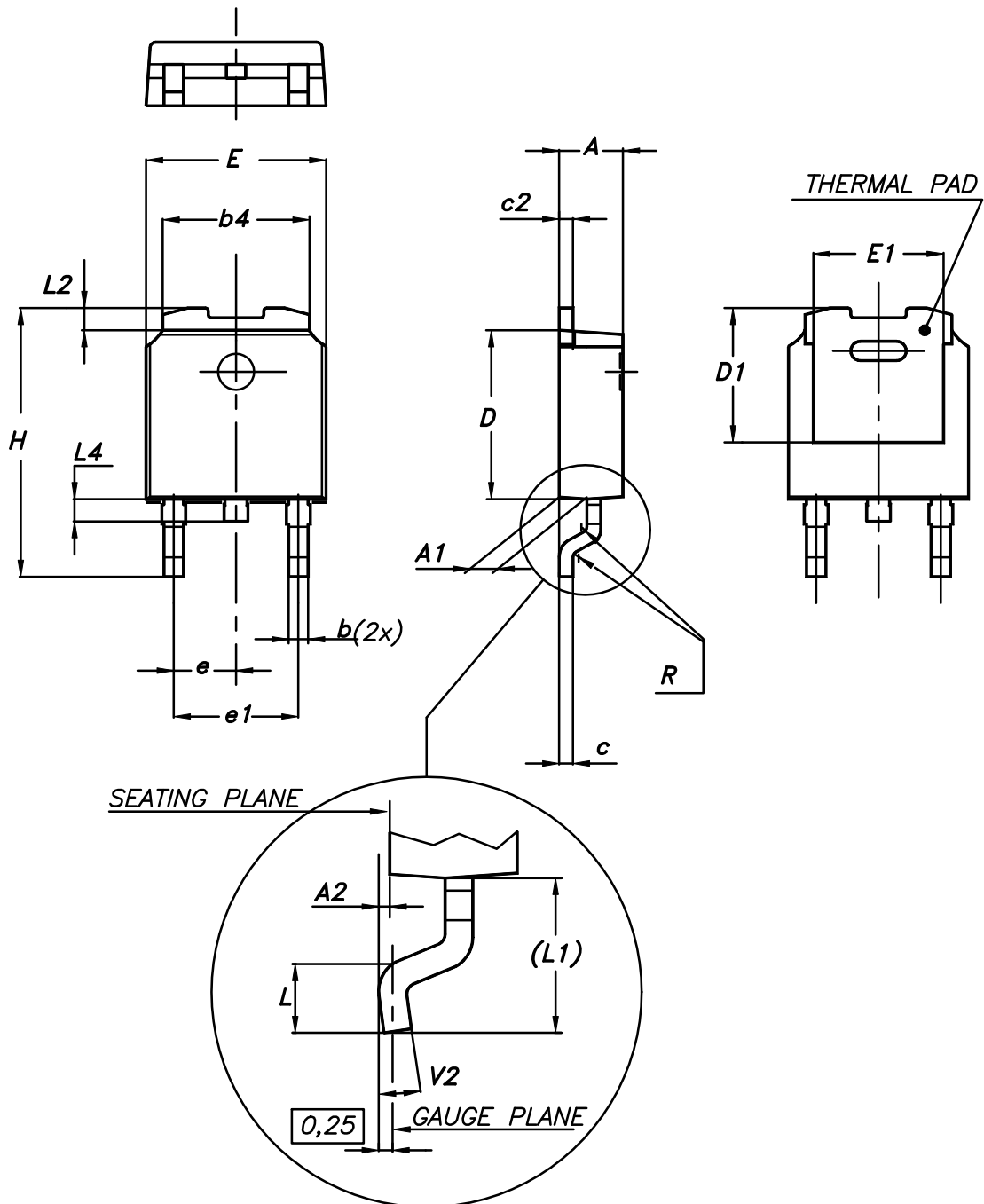
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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 18. DPAK (TO-252) type A package outline



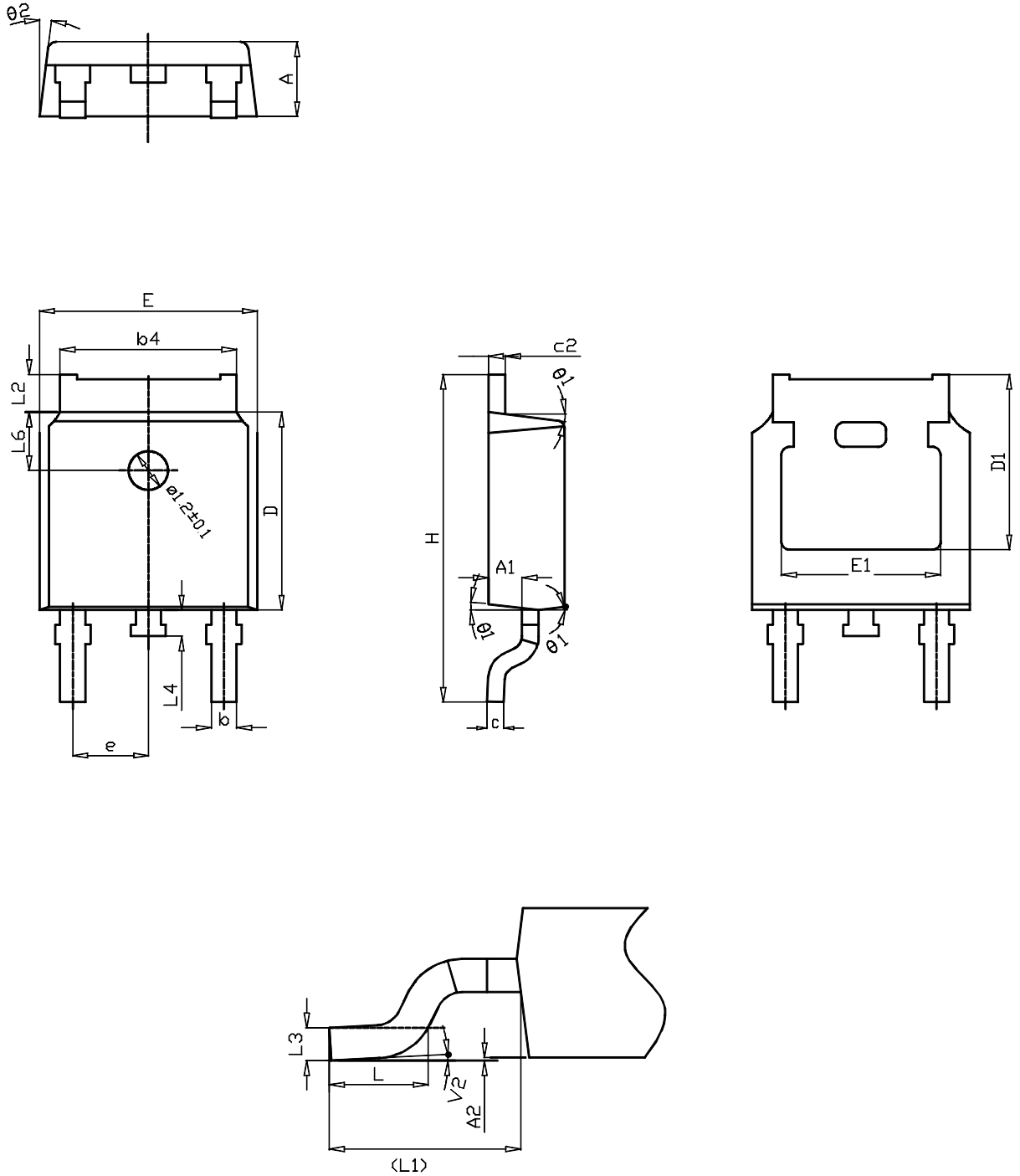
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Table 7. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

4.2 DPAK (TO-252) type C package information

Figure 19. DPAK (TO-252) type C package outline



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Table 8. DPAK (TO-252) type C mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

4.3 DPAK (TO-252) type E package information

Figure 20. DPAK (TO-252) type E package outline

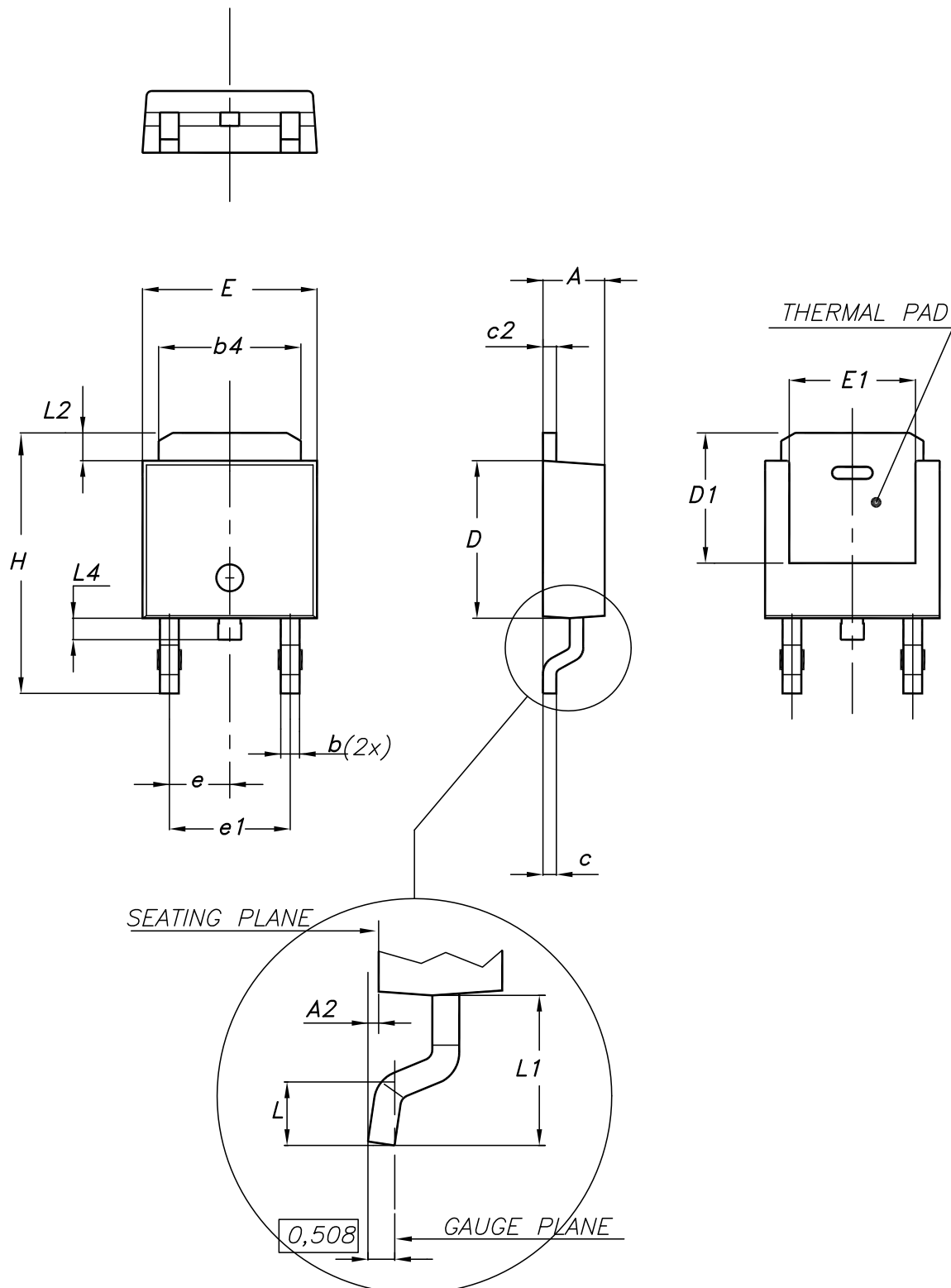
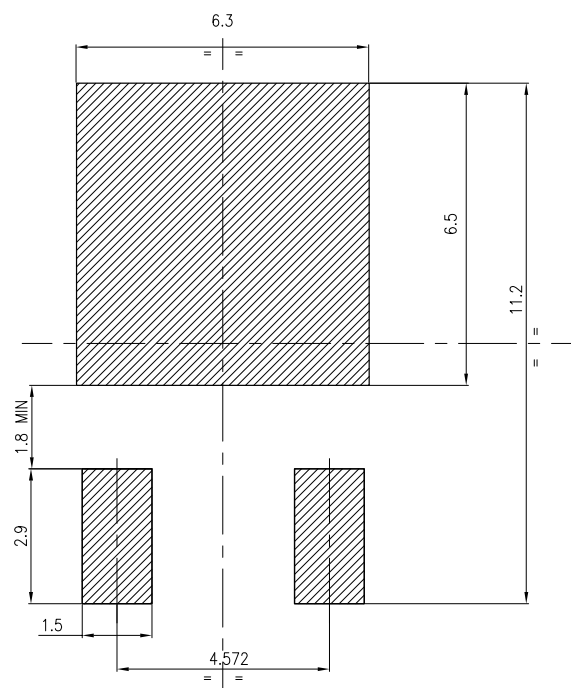


Table 9. DPAK (TO-252) type E mechanical data

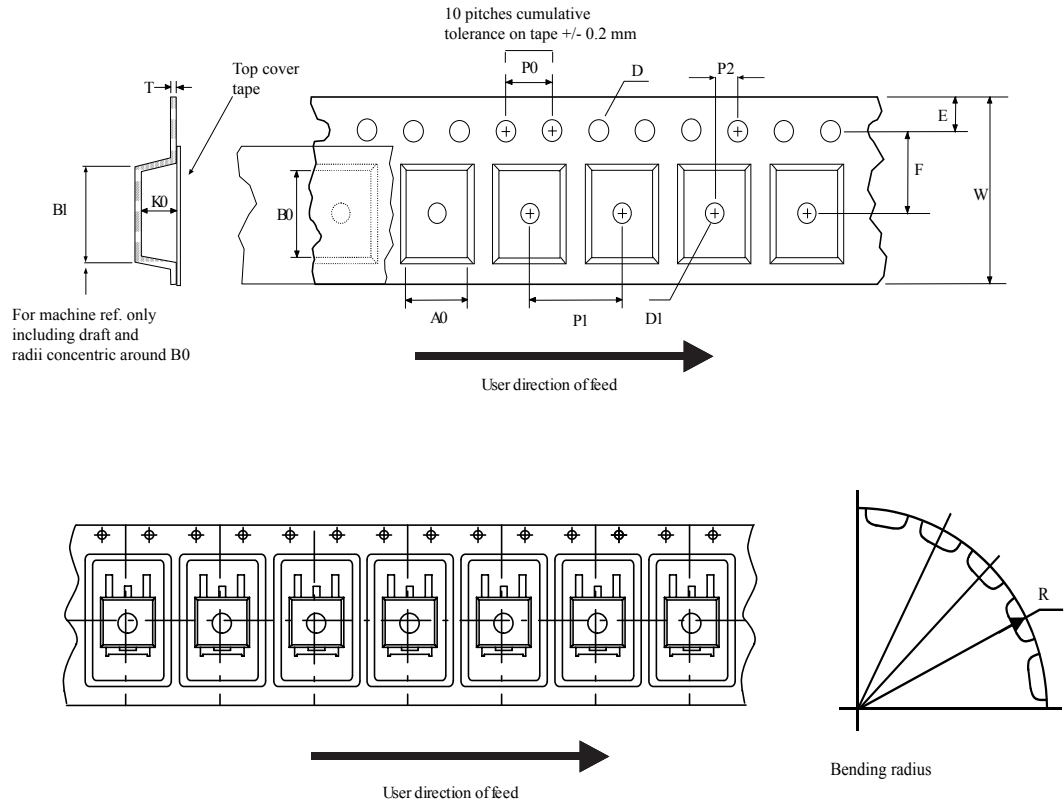
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

Figure 21. DPAK (TO-252) recommended footprint (dimensions are in mm)


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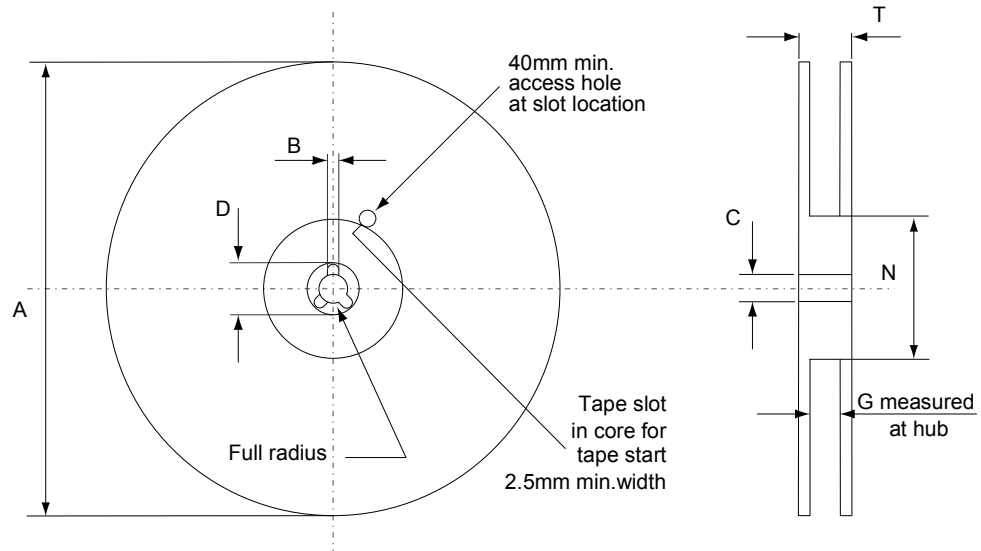
4.4 DPAK (TO-252) packing information

Figure 22. DPAK (TO-252) tape outline



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Figure 23. DPAK (TO-252) reel outline



AM06038v1

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Revision history

Table 11. Document revision history

Date	Version	Changes
26-Jun-2014	1	First release.
14-Nov-2014	2	Updated title and features in cover page Updated <i>Table 3: Thermal data</i> , <i>Table 4: On/off states</i> and <i>Table 5:Dynamic</i> . Updated <i>Figure 2: Safe operating area</i> , <i>Figure 3: Thermal impedance</i> , <i>Figure 6: Normalized V(BR)DSS vs. temperature</i> , <i>Figure 10</i> , <i>Figure 11: Normalized on-resistance vs. temperature</i> and <i>Section 4: Package mechanical data</i> .
09-Aug-2018	3	Removed maturity status indication from cover page. The document status is production data. Updated title and features on cover page. Updated Section 4 Package information . Minor text changes

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4.4	DPAK (TO-252) packing information	14
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