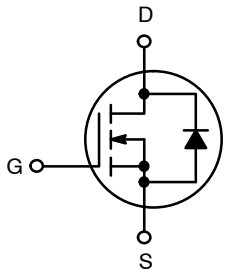
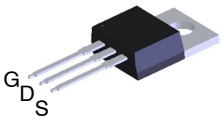
MOSFET – N-Channel, UniFET™

500 V, 18 A, 265 mΩ

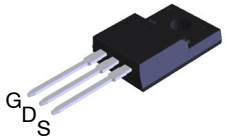
FDP18N50 / FDPF18N50 / FDPF18N50T

V_{DS}	$R_{DS(ON)}$ MAX	I_D MAX
500 V	265 mΩ @ 9 V	18 A





TO−220−3LD
CASE 340AT



TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT

Description

UniFET MOSFET is **onsemi**'s high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on−state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)}$ = 220 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 9 A
- Low Gate Charge (Typ. 45 nC)
- Low C_{rss} (Typ. 25 pF)
- 100% Avalanche Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- LCD/LED/PDP TV
- Lighting
- Uninterruptible Power Supply

MARKING DIAGRAM

FDP18N50,
FDPF18N50
FDPF18N50T = Specific Device Code
A = Assembly Location
YWW = Date Code (Year and Week)
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping
FDP18N50	TO−220	1000 Units / Tube
FDPF18N50	TO−220F	1000 Units / Tube
FDPF18N50T	TO−220F	1000 Units / Tube

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDP18N50	FDPF18N50 / FDPF18N50T	Unit
V_{DSS}	Drain to Source Voltage		500		V
I_D	Drain Current –	– Continuous (T_C = 25°C) – Continuous (T_C = 100°C)	18 10.8	18* 10.8*	A
I_{DM}	Drain Current	– Pulsed (Note 1)	72	72*	A
V_{GSS}	Gate to Source Voltage		±30		V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		945		mJ
I_{AR}	Avalanche Current (Note 1)		18		A
E_{AR}	Repetitive Avalanche Energy (Note 1)		23.5		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
P_D	Power Dissipation	(T_C = 25°C) – Derate Above 25°C	235 1.88	38.5 0.3	W W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		–55 to +150		°C
T_L	Maximum Lead Temperature for Soldering, 1/8″ from Case for 5 Second		300		°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Drain current limited by maximum junction temperature
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. L = 5.2 mH, I_{AS} = 18 A, V_{DD} = 50 V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ 18 A, di/dt ≤ 200 A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C

THERMAL CHARACTERISTICS

Symbol	Parameter	FDP18N50	FDPF18N50 / FDPF18N50T	Unit
$R_{\theta JC}$	Thermal Resistance, Junction–to–Case, Max.	0.53	3.3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction–to–Ambient, Max.	62.5	62.5	°C/W

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain–Source Breakdown Voltage	V_{GS} = 0, I_D = 250 μA,	500	–	–	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.5	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 400 V, T_C = 125°C	–	–	10	
I_{GSSF}	Gate–Body Leakage Current, Forward	V_{GS} = 30 V, V_{DS} = 0 V	–	–	100	nA
I_{GSSR}	Gate–Body Leakage Current, Reserve	V_{GS} = –30 V, V_{DS} = 0 V	–	–	–100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 9 A	–	0.220	0.265	Ω
g_{FS}	Forward Transconductance	V_{DS} = 40 V, I_D = 9 A	–	25	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	2200	2860	pF
C_{oss}	Output Capacitance		–	330	430	pF
C_{rss}	Reverse Transfer Capacitance		–	25	40	pF

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = 250 V, I_D = 18 A, V_{GS} = 10 V,R_G = 25 Ω (Note 4)	−	55	120	ns
t_r	Turn−On Rise Time		−	165	340	ns
$t_{d(off)}$	Turn−Off Delay Time		−	95	200	ns
t_f	Turn−Off Fall Time		−	90	190	ns
Q_g	Total Gate Charge	V_{DS} = 400 V, I_D = 18 A, V_{GS} = 10 V (Note 4)	−	45	60	nC
Q_{gs}	Gate−Source Charge		−	12.5	−	nC
Q_{gd}	Gate−Drain Charge		−	19	−	nC
DRAIN−SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	18	A
I_{SM}	Maximum Pulsed Drain− Source Diode Forward Current		−	−	72	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 18 A	−	−	1.4	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 18 A dI_F/dt = 100 A/μs	−	500	−	ns
Q_{rr}	Reverse Recovery Charge		−	5.4	−	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially Independent of Operating Temperature Typical Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS

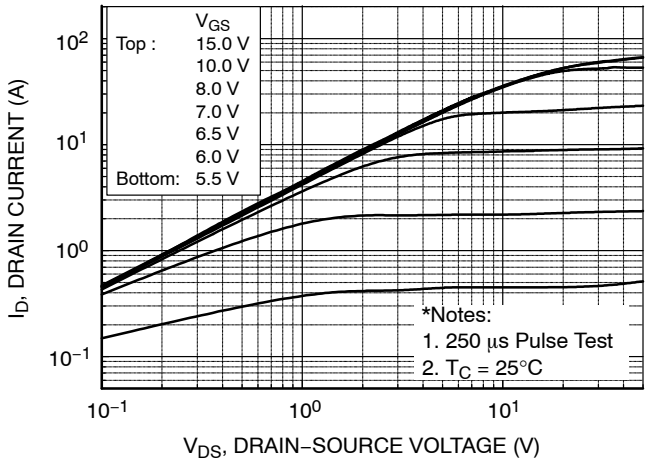


Figure 1. On−Resistance Characteristics

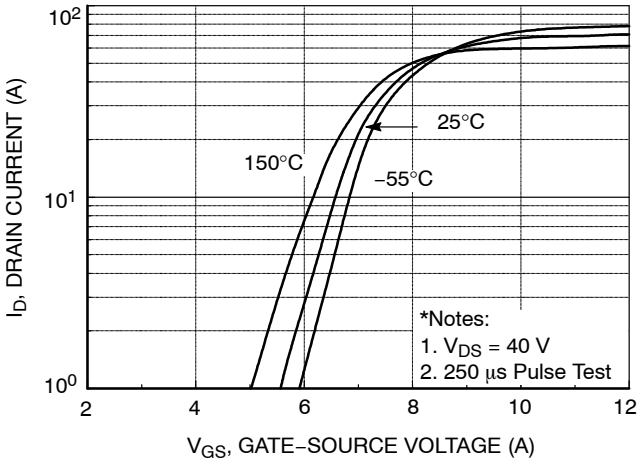


Figure 2. Transfer Characteristics

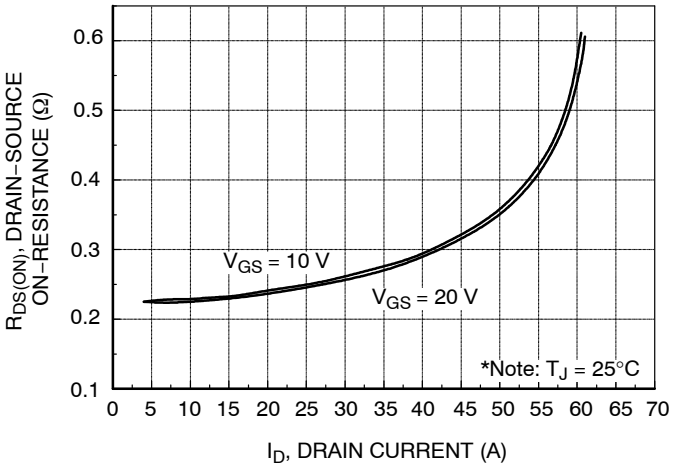


Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage

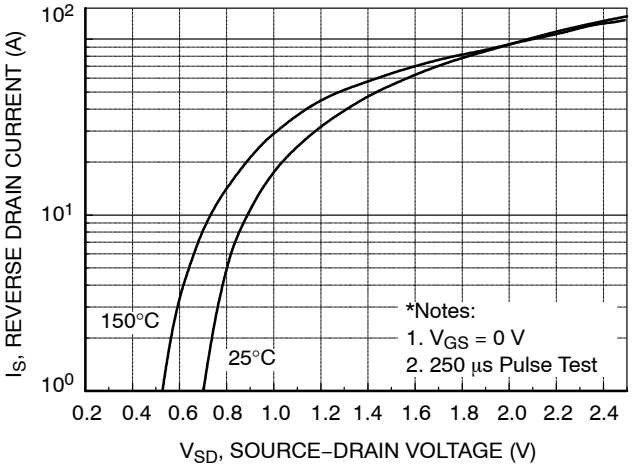


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

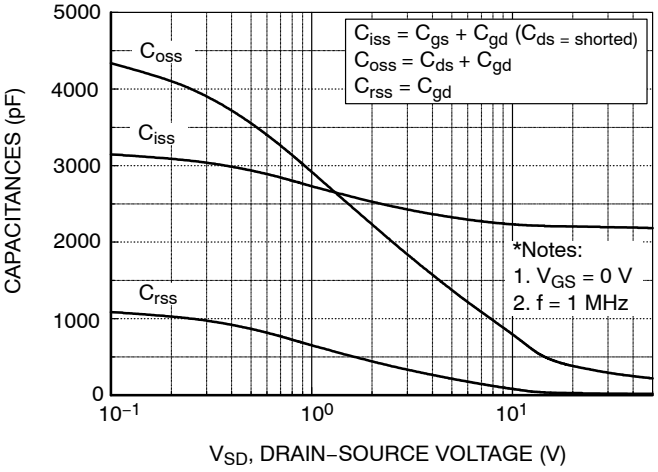


Figure 5. Capacitance Characteristics

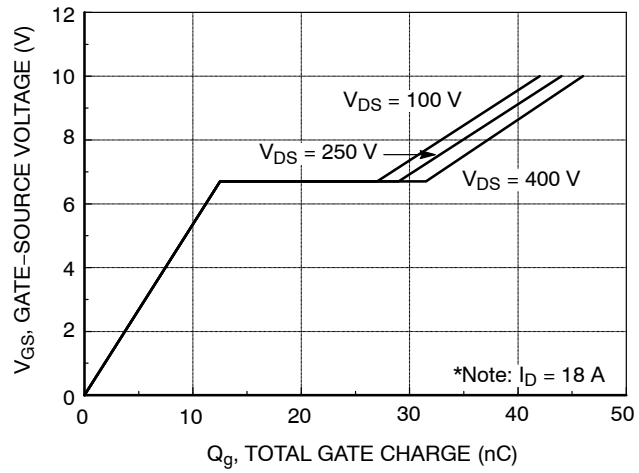


Figure 6. Gate Charge Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

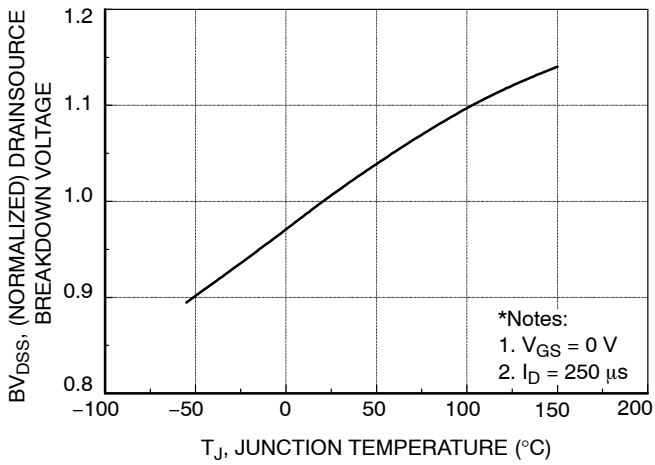


Figure 7. Breakdown Voltage Variation vs. Temperature

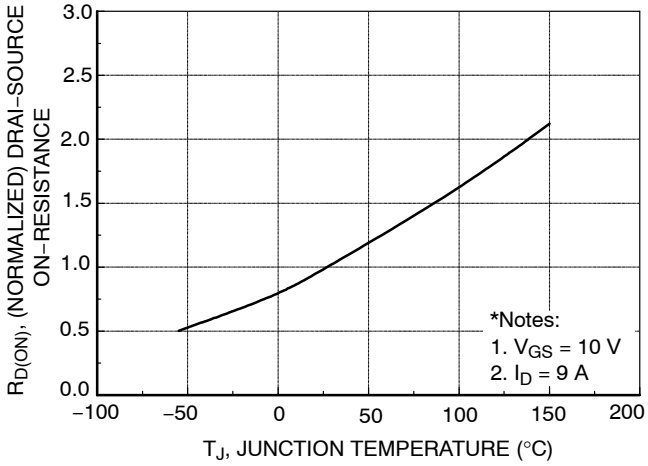


Figure 8. On−Resistance Variation vs. Temperature

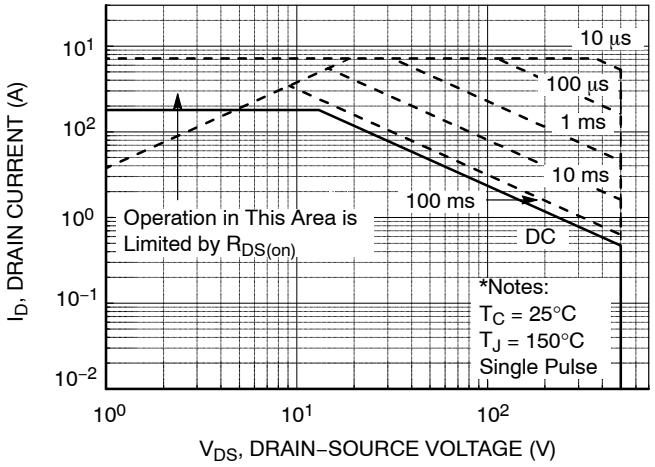


Figure 9−1. Maximum Safe Operating Area for FDP18N50

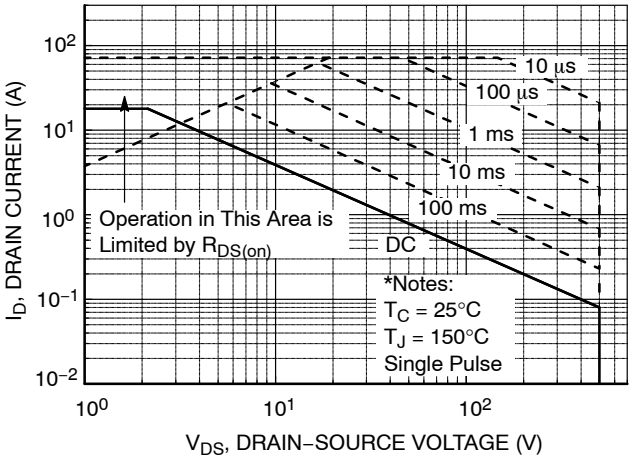


Figure 9−2. Maximum Safe Operating Area for FDPF18N50 / FDPF18N50T

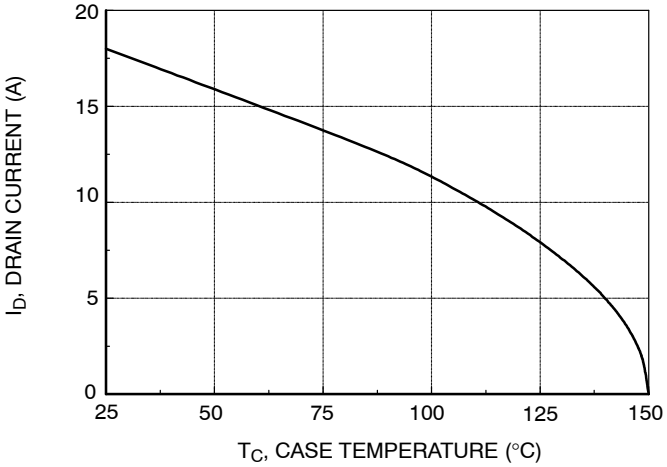


Figure 10. Maximum Drain Current vs. Case Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

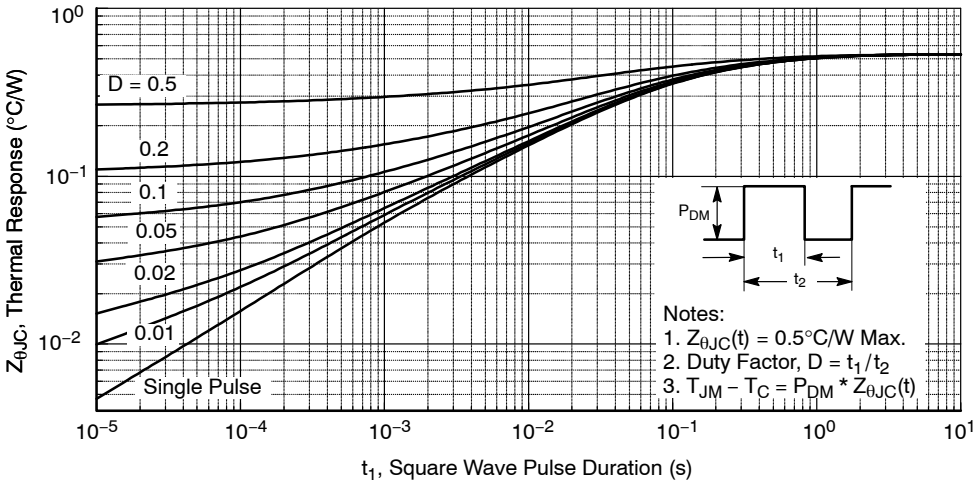


Figure 11 –1. Transient Thermal Response Curve – FDP18N50

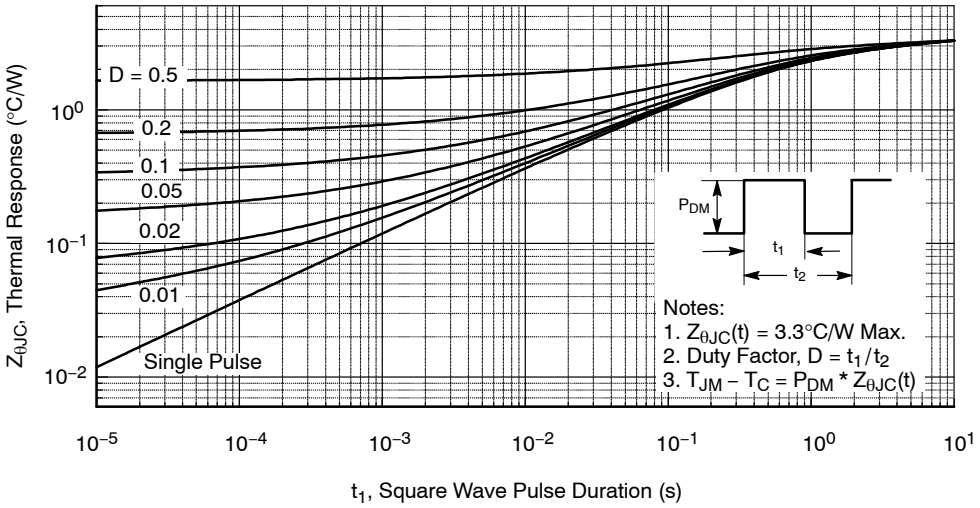


Figure 11 –2. Transient Thermal Response Curve – FDPF18N50 / FDPF18N50T

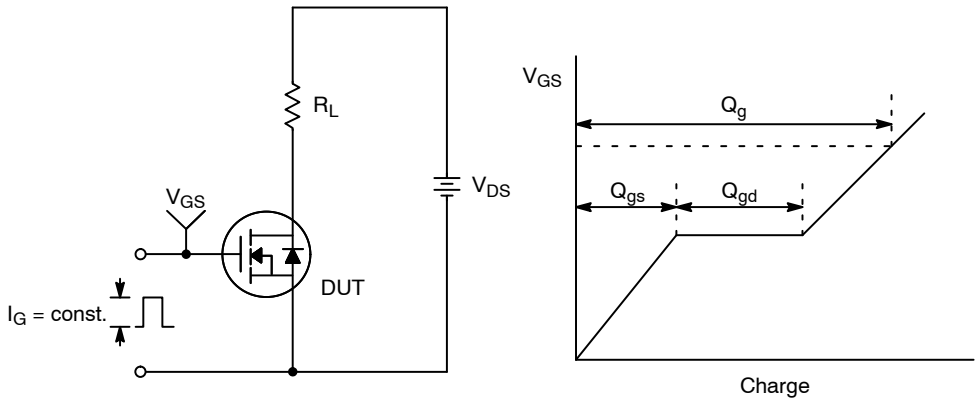


Figure 12. Gate Charge Test Circuit & Waveform

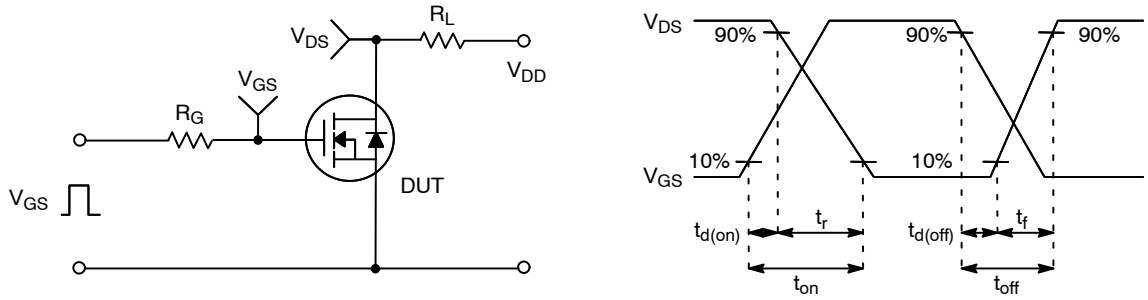


Figure 13. Resistive Switching Test Circuit & Waveforms

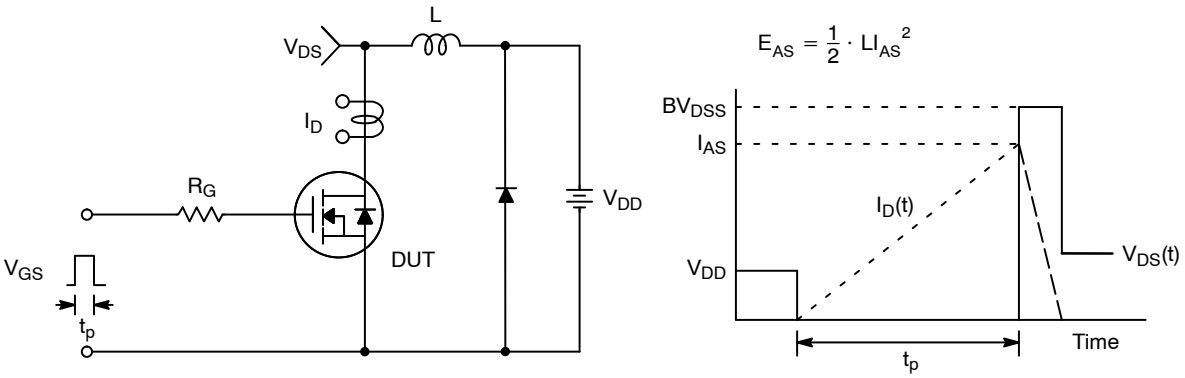


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

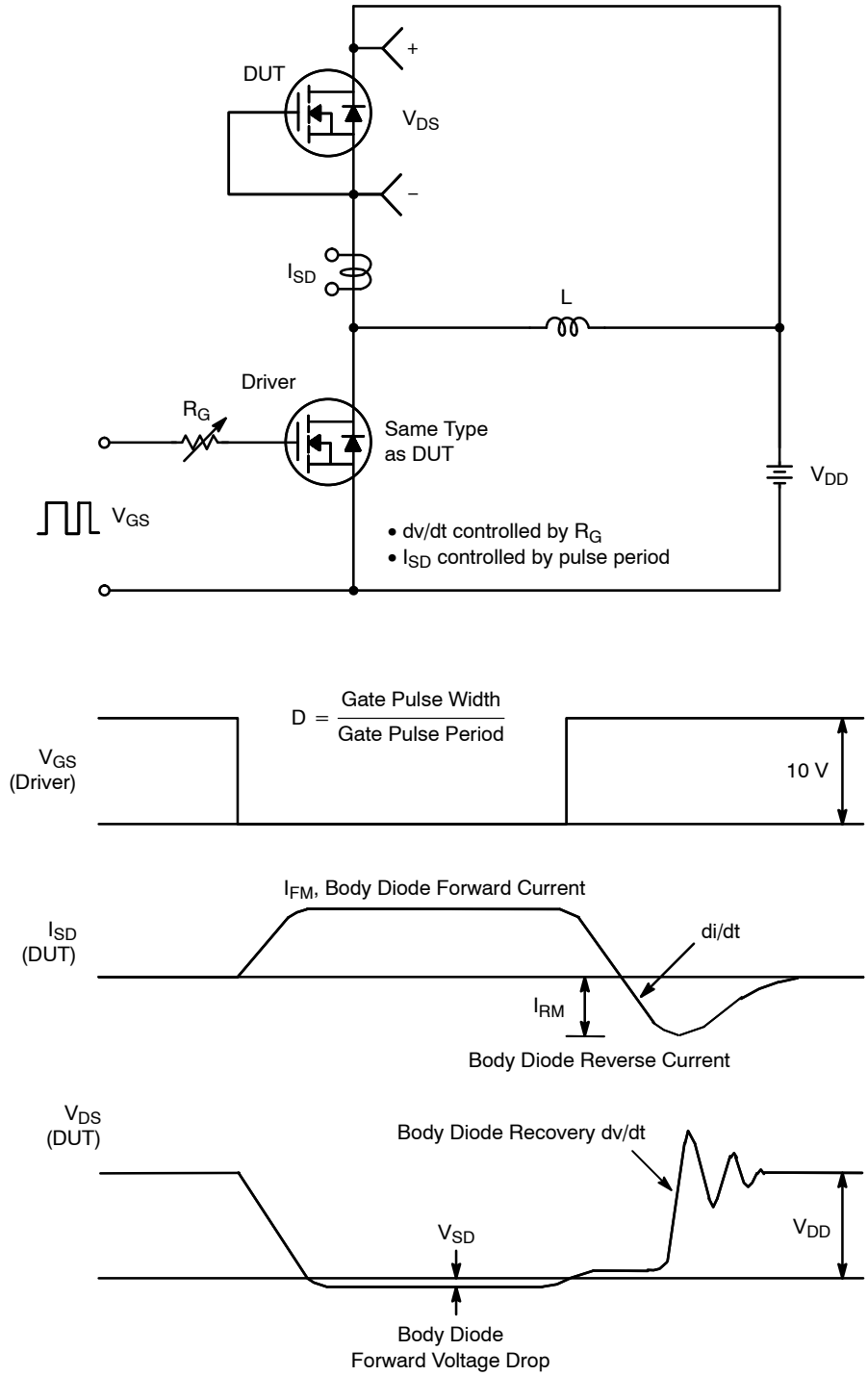
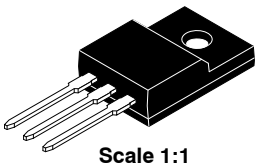


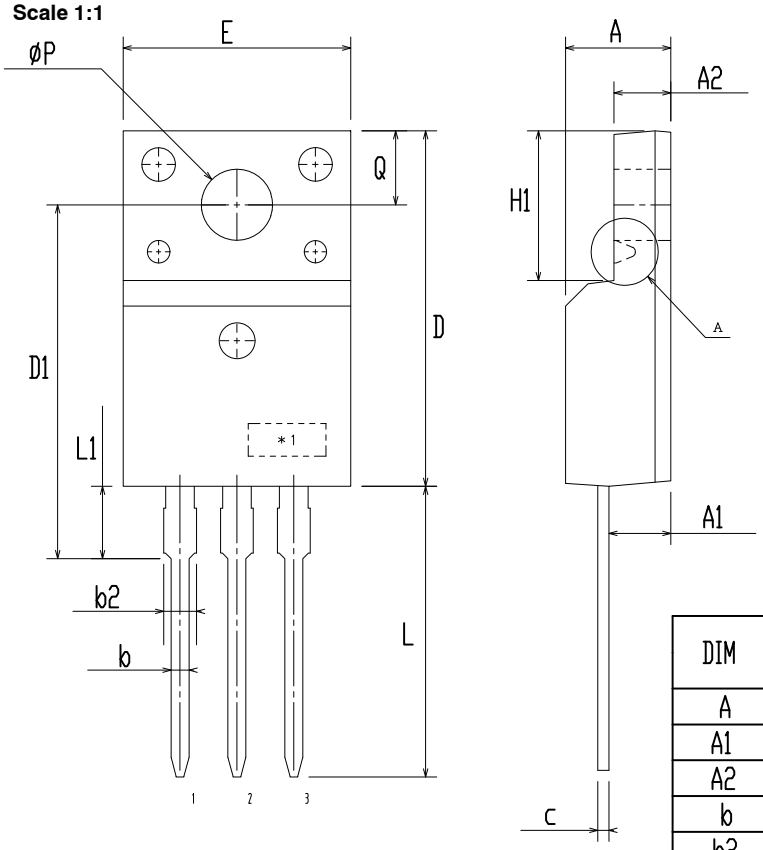
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

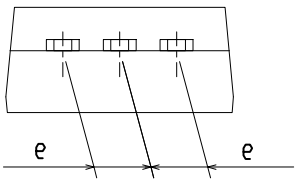
TO−220 Fullpack, 3−Lead / TO−220F−3SG
CASE 221AT
ISSUE B

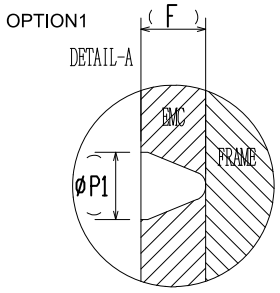
DATE 19 JAN 2021



Scale 1:1







DIM	MILLIMITERS		
	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.56	2.76	2.96
A2	2.34	2.54	2.74
b	0.70	0.80	0.90
b2	~	~	1.47
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.60	15.80	16.00
E	9.96	10.16	10.36
e	2.34	2.54	2.74
F	~	0.84	~
H1	6.48	6.68	6.88
L	12.78	12.98	13.18
L1	3.03	3.23	3.43
ø P	2.98	3.18	3.38
ø P1	~	1.00	~
Q	3.20	3.30	3.40

NOTES:
A. DIMENSION AND TOLERANCE AS ASME Y14.5-2009
B. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUCSIONS.
C. OPTION 1 - WITH SUPPORT PIN HOLE
OPTION 2 - NO SUPPORT PIN HOLE

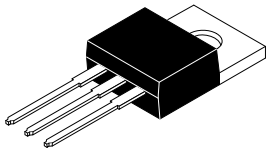
DOCUMENT NUMBER:	**98AON67439E**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−220 FULLPACK, 3−LEAD / TO−220F−3SG**	**PAGE 1 OF 1**

MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

ON Semiconductor®

TO−220−3LD
CASE 340AT
ISSUE A

DATE 03 OCT 2017



Scale 1:1

NOTES:
A) REFERENCE JEDEC, TO-220, VARIATION AB
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS COMMON TO ALL PACKAGE SUPPLIERS EXCEPT WHERE NOTED [ ].
D) LOCATION OF MOLDED FEATURE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
E DOES NOT COMPLY JEDEC STANDARD VALUE.
F) "A1" DIMENSIONS AS BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1.10 - 1.45
G PRESENCE IS SUPPLIER DEPENDENT
H) SUPPLIER DEPENDENT MOLD LOCKING HOLES IN HEATSINK.

DOCUMENT NUMBER:	**98AON13818G**	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	**TO−220−3LD**	**PAGE 1 OF 1**

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support
For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales