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# FAIRCHILD

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# FQP5N50C/FQPF5N50C 500V N-Channel MOSFET

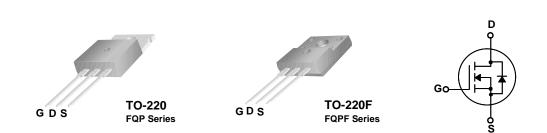
### **General Description**

These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar stripe, DMOS technology.

This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switched mode power supplies, active power factor correction, electronic lamp ballasts based on half bridge topology.

#### Features

- 5A, 500V, R<sub>DS(on)</sub> = 1.4 Ω @V<sub>GS</sub> = 10 V
- Low gate charge (typical 18nC)
- Low Crss (typical 15pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



## Absolute Maximum Ratings T<sub>c</sub> = 25°C unless otherwise noted

Symbol	Parameter		FQP5N50C	FQPF5N50C	Units
V <sub>DSS</sub>	Drain-Source Voltage		500		V
I <sub>D</sub>	Drain Current - Continuous ( $T_C = 25^{\circ}C$ )		5	5 *	А
	- Continuous (T <sub>C</sub> = 100°C)		2.9	2.9 *	А
I <sub>DM</sub>	Drain Current - Pulsed	(Note 1)	20	20 *	А
V <sub>GSS</sub>	Gate-Source Voltage		± 30		V
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)		300		mJ
I <sub>AR</sub>	Avalanche Current	(Note 1)	5		А
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)		7.3		mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5		V/ns
PD	Power Dissipation ( $T_C = 25^{\circ}C$ )		73	38	W
	- Derate above 25°C		0.58	0.3	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range		-55 to +150		°C
т	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300		°C
Τ <sub>L</sub>					
Drain current lim	nited by maximum junction temperature				

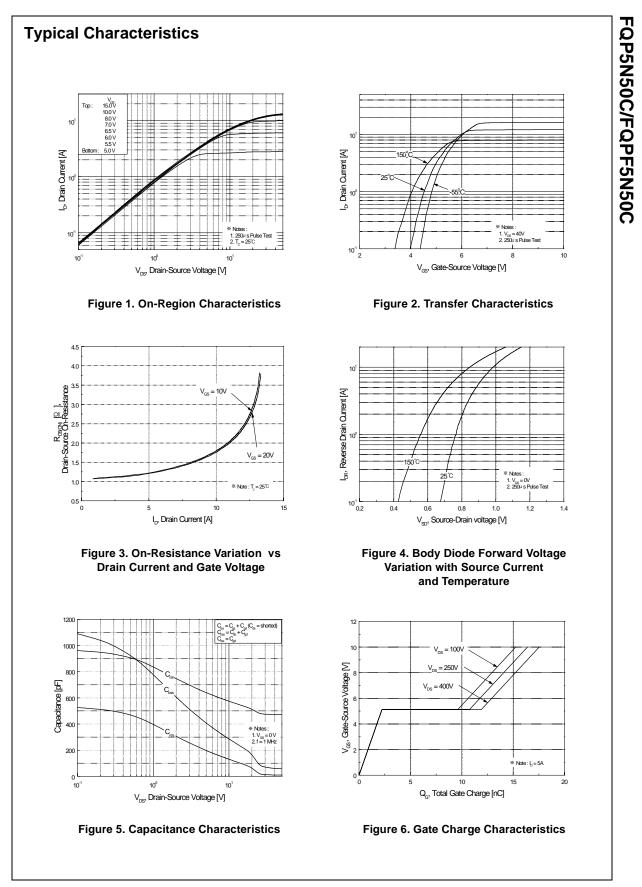
## **Thermal Characteristics**

Symbol	Parameter	FQP5N50C	FQPF5N50C	Units
$R_{ extsf{ heta}JC}$	Thermal Resistance, Junction-to-Case	1.71	3.31	°C/W
$R_{ extsf{ heta}JS}$	Thermal Resistance, Case-to-Sink Typ.	0.5		°C/W
$R_{ extsf{ heta}JA}$	Thermal Resistance, Junction-to-Ambient	62.5	62.5	°C/W

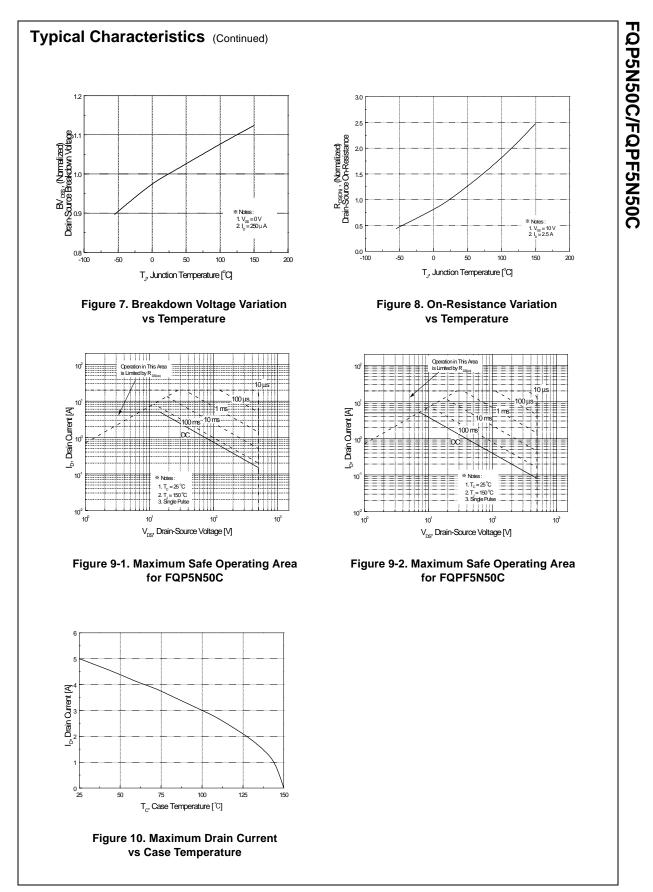
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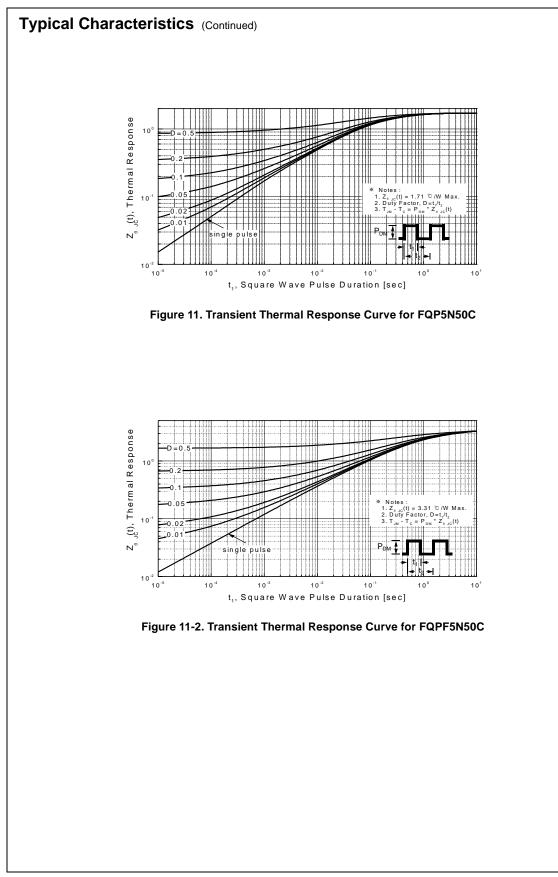
**FET**<sup>™</sup>

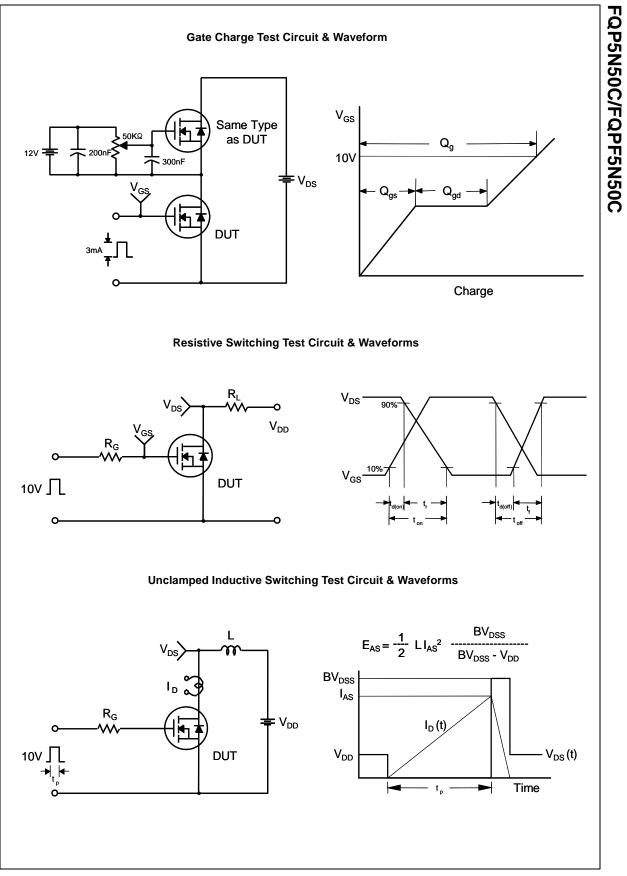
Symbol	Parameter	Test Conditions		Min	Тур	Max	Units
Off Cha	aracteristics						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 V, I_{D} = 250 \mu A$		500			V
ΔBV <sub>DSS</sub> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = 250 \ \mu A$ , Referenced	to 25°C		0.5		V/°C
IDSS	Zero Gate Voltage Drain Current	$V_{DS} = 500 \text{ V}, \text{ V}_{GS} = 0 \text{ V}$				1	μA
		V <sub>DS</sub> = 400 V, T <sub>C</sub> = 125°C	;			10	μA
GSSF	Gate-Body Leakage Current, Forward	$V_{GS} = 30 \text{ V}, V_{DS} = 0 \text{ V}$				100	nA
GSSR	Gate-Body Leakage Current, Reverse	$V_{GS} = -30 \text{ V}, \text{ V}_{DS} = 0 \text{ V}$				-100	nA
On Cha	racteristics						
/ <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$		2.0		4.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, \text{ I}_{D} = 2.5 \text{ A}$			1.14	1.4	Ω
ĴFS	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_{D} = 2.5 \text{ A}$	(Note 4)		5.2		S
	ic Characteristics						
S <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			480	625	pF
C <sub>oss</sub>	Output Capacitance				80	105	pF
Srss	Reverse Transfer Capacitance				15	20	pF
Switchi	ing Characteristics						
d(on)	Turn-On Delay Time	$V_{DD} = 250 \text{ V}, \text{ I}_D = 5\text{A},$ $R_G = 25 \Omega$			12	35	ns
r	Turn-On Rise Time				46	100	ns
d(off)	Turn-Off Delay Time				50	110	ns
f	Turn-Off Fall Time		(Note 4, 5)	-	48	105	ns
ζ <sup>g</sup>	Total Gate Charge	$V_{DS} = 400 \text{ V}, I_{D} = 5\text{A},$			18	24	nC
ב <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V			2.2		nC
ຊ <sub>gd</sub>	Gate-Drain Charge		(Note 4, 5)		9.7		nC
Drain-S	ource Diode Characteristics ar	nd Maximum Ratings	S				
S	Maximum Continuous Drain-Source Dic	ode Forward Current				5	Α
SM	Maximum Pulsed Drain-Source Diode F	Forward Current				20	Α
/ <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 V, I_{S} = 5 A$				1.4	V
rr	Reverse Recovery Time	$V_{GS} = 0 V, I_{S} = 5 A,$			263		ns
ל <sup>גע</sup>	Reverse Recovery Charge	dI <sub>F</sub> / dt = 100 A/µs	(Note 4)		1.9		μC
L ≕ 21.5 m I <sub>SD</sub> ≤ 5A, di	ating : Pulse width limited by maximum junction temper H, I <sub>AS</sub> = 5A, V <sub>DD</sub> = 50V, R <sub>G</sub> = 25 \Omega, Starting T <sub>J</sub> = 25°C /dt $\leq$ 200A/µs, V <sub>DD</sub> $\leq$ BV <sub>DSS</sub> , Starting T <sub>J</sub> = 25°C Pulse width $\leq$ 300µs, Duty cycle $\leq$ 2%						

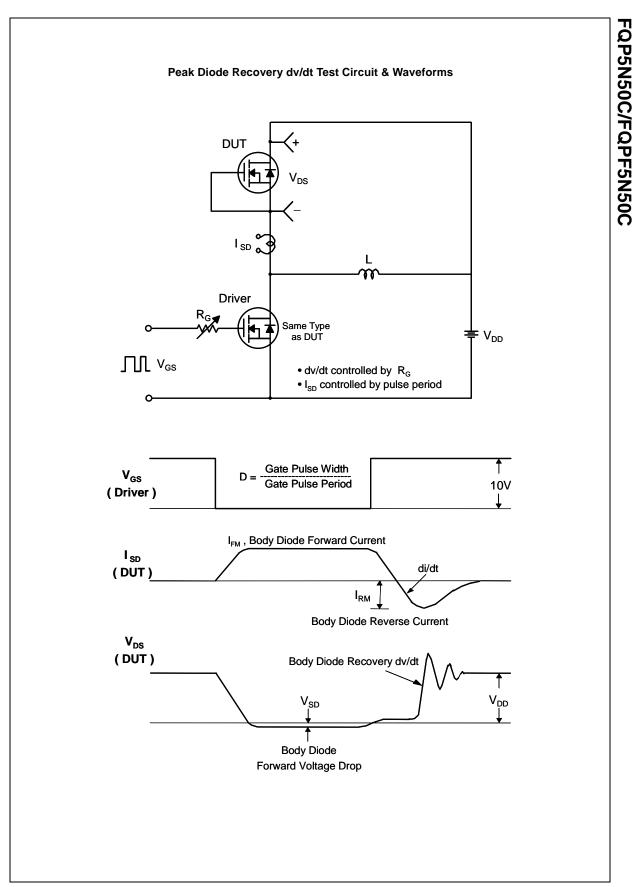


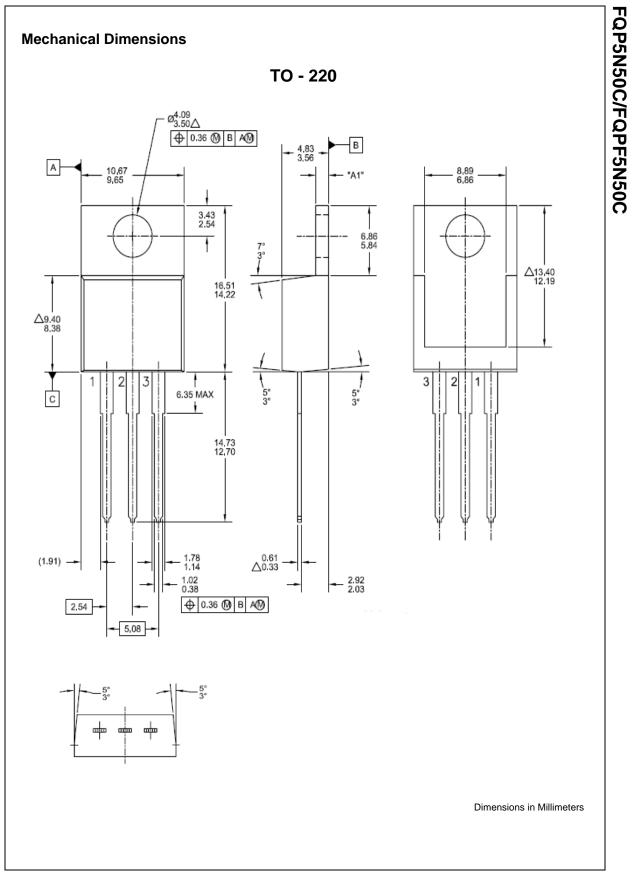
Rev. A, April 2003



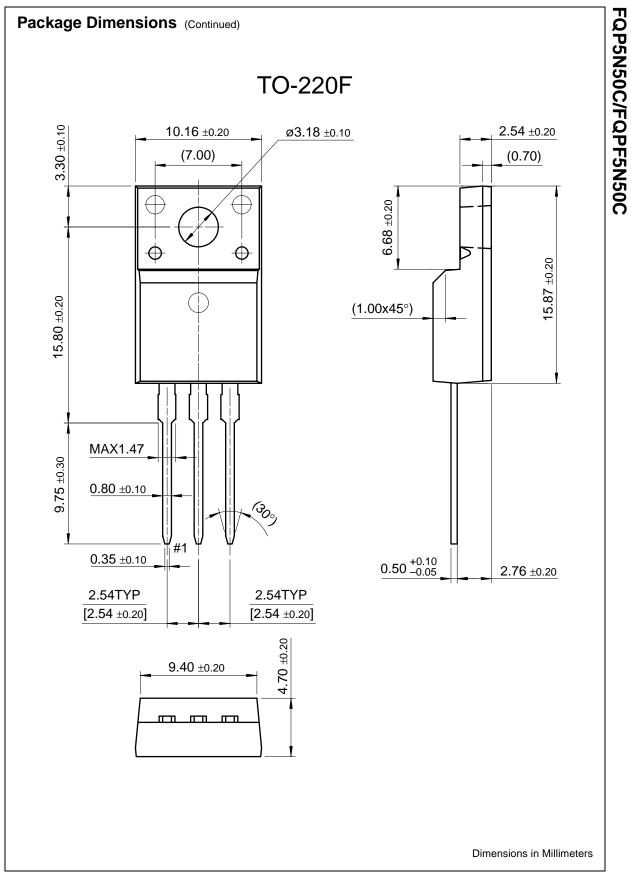








Rev. A, April 2003



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