



RF Power Field Effect Transistors

N-Channel Enhancement-Mode Lateral MOSFETs

Designed for broadband commercial and industrial applications with frequencies to 520 MHz. The high gain and broadband performance of these devices make them ideal for large-signal, common source amplifier applications in 12.5 volt mobile FM equipment.

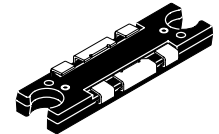
- Specified Performance @ 520 MHz, 12.5 Volts
 Output Power — 35 Watts
 Power Gain — 13.5 dB
 Efficiency — 55%
- Capable of Handling 20:1 VSWR, @ 15.6 Vdc, 520 MHz, 2 dB Overdrive

Features

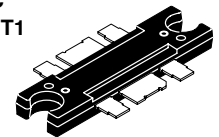
- Excellent Thermal Stability
- Characterized with Series Equivalent Large-Signal Impedance Parameters
- Broadband-Full Power Across the Band: 135-175 MHz
 400-470 MHz
 450-520 MHz
- 200°C Capable Plastic Package
- N Suffix Indicates Lead-Free Terminations. RoHS Compliant.
- In Tape and Reel. T1 Suffix = 500 Units per 44 mm, 13 inch Reel.

MRF1535NT1
MRF1535FNT1

520 MHz, 35 W, 12.5 V
LATERAL N-CHANNEL
BROADBAND
RF POWER MOSFETs



CASE 1264-10, STYLE 1
TO-272-6 WRAP
PLASTIC
MRF1535NT1



CASE 1264A-03, STYLE 1
TO-272-6
PLASTIC
MRF1535FNT1

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain-Source Voltage	V _{DSS}	-0.5, +40	Vdc
Gate-Source Voltage	V _{GS}	±20	Vdc
Drain Current — Continuous	I _D	6	Adc
Total Device Dissipation @ T _C = 25°C (1) Derate above 25°C	P _D	135 0.50	W W/°C
Storage Temperature Range	T _{stg}	- 65 to +150	°C
Operating Junction Temperature	T _J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value(2)	Unit
Thermal Resistance, Junction to Case	R _{θJC}	0.90	°C/W

Table 3. Moisture Sensitivity Level

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD 22-A113, IPC/JEDEC J-STD-020	1	260	°C

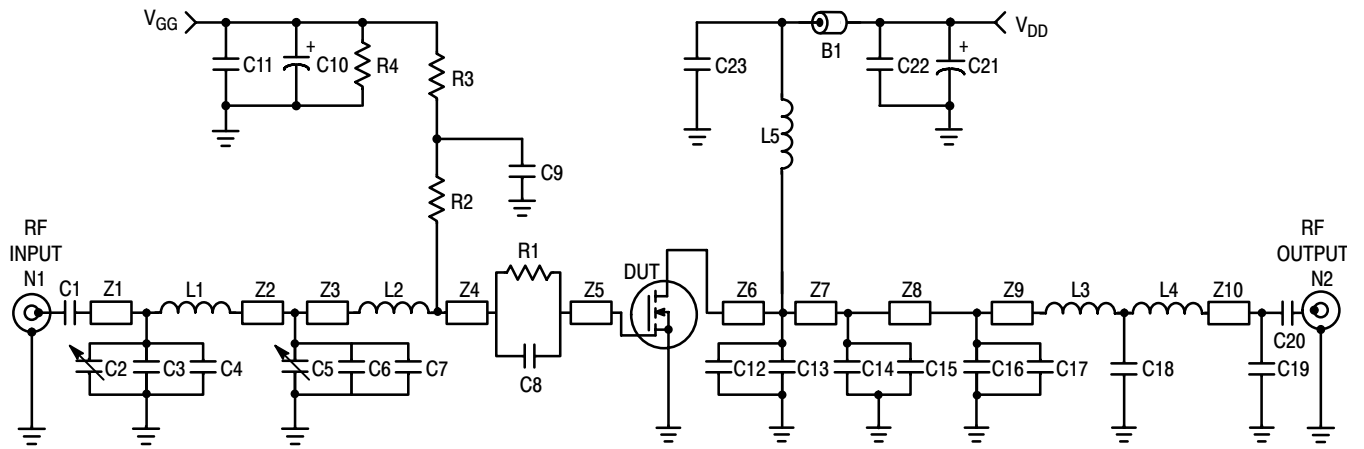
1. Calculated based on the formula $P_D = \frac{T_J - T_C}{R_{\theta JC}}$

2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.

NOTE - CAUTION - MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.

Table 4. Electrical Characteristics ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Drain-Source Breakdown Voltage ($V_{GS} = 0\text{ Vdc}$, $I_D = 100\ \mu\text{Adc}$)	$V_{(BR)DSS}$	60	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 60\text{ Vdc}$, $V_{GS} = 0\text{ Vdc}$)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current ($V_{GS} = 10\text{ Vdc}$, $V_{DS} = 0\text{ Vdc}$)	I_{GSS}	—	—	0.3	μAdc
On Characteristics					
Gate Threshold Voltage ($V_{DS} = 12.5\text{ Vdc}$, $I_D = 400\ \mu\text{A}$)	$V_{GS(th)}$	1	—	2.6	Vdc
Drain-Source On-Voltage ($V_{GS} = 5\text{ Vdc}$, $I_D = 0.6\text{ A}$)	$R_{DS(on)}$	—	—	0.7	Ω
Drain-Source On-Voltage ($V_{GS} = 10\text{ Vdc}$, $I_D = 2.0\text{ Adc}$)	$V_{DS(on)}$	—	—	1	Vdc
Dynamic Characteristics					
Input Capacitance (Includes Input Matching Capacitance) ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{iss}	—	—	250	pF
Output Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{oss}	—	—	150	pF
Reverse Transfer Capacitance ($V_{DS} = 12.5\text{ Vdc}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$)	C_{rss}	—	—	20	pF
RF Characteristics (In Freescale Test Fixture)					
Common-Source Amplifier Power Gain ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 35\text{ Watts}$, $I_{DQ} = 500\text{ mA}$) $f = 520\text{ MHz}$	G_{ps}	—	13.5	—	dB
Drain Efficiency ($V_{DD} = 12.5\text{ Vdc}$, $P_{out} = 35\text{ Watts}$, $I_{DQ} = 500\text{ mA}$) $f = 520\text{ MHz}$	η	—	55	—	%



B1	Ferroxcube #VK200	L4	1 Turn, #26 AWG, 0.240" ID
C1, C9, C20, C23	330 pF, 100 mil Chip Capacitors	L5	4 Turn, #24 AWG, 0.180" ID
C2, C5	0 to 20 pF Trimmer Capacitors	N1, N2	Type N Flange Mounts
C3, C15	33 pF, 100 mil Chip Capacitors	R1	6.5 Ω , 1/4 W Chip Resistor
C4, C6, C19	18 pF, 100 mil Chip Capacitors	R2	39 Ω Chip Resistor (0805)
C7	160 pF, 100 mil Chip Capacitor	R3	1.2 k Ω , 1/8 W Chip Resistor
C8	240 pF, 100 mil Chip Capacitor	R4	33 k Ω , 1/4 W Chip Resistor
C10, C21	10 μ F, 50 V Electrolytic Capacitors	Z1	0.970" x 0.080" Microstrip
C11, C22	470 pF, 100 mil Chip Capacitors	Z2	0.380" x 0.080" Microstrip
C12, C13	150 pF, 100 mil Chip Capacitors	Z3	0.190" x 0.080" Microstrip
C14	110 pF, 100 mil Chip Capacitor	Z4	0.160" x 0.080" Microstrip
C16	68 pF, 100 mil Chip Capacitor	Z5, Z6	0.110" x 0.200" Microstrip
C17	120 pF, 100 mil Chip Capacitor	Z7	0.490" x 0.080" Microstrip
C18	51 pF, 100 mil Chip Capacitor	Z8	0.250" x 0.080" Microstrip
L1	17.5 nH, Coilcraft #A05T	Z9	0.320" x 0.080" Microstrip
L2	5 nH, Coilcraft #A02T	Z10	0.240" x 0.080" Microstrip
L3	1 Turn, #26 AWG, 0.250" ID	Board	Glass Teflon [®] , 31 mils

Figure 1. 135 - 175 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 135 - 175 MHz

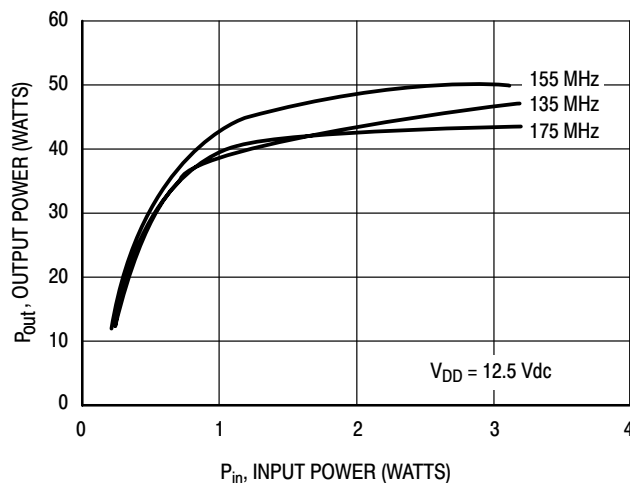


Figure 2. Output Power versus Input Power

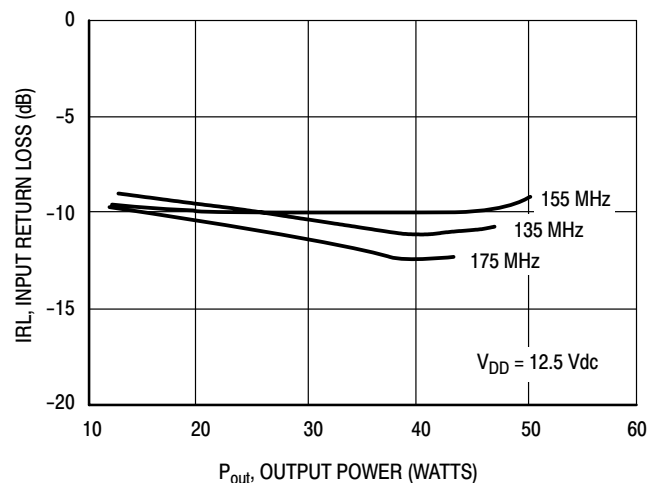


Figure 3. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 135 - 175 MHz

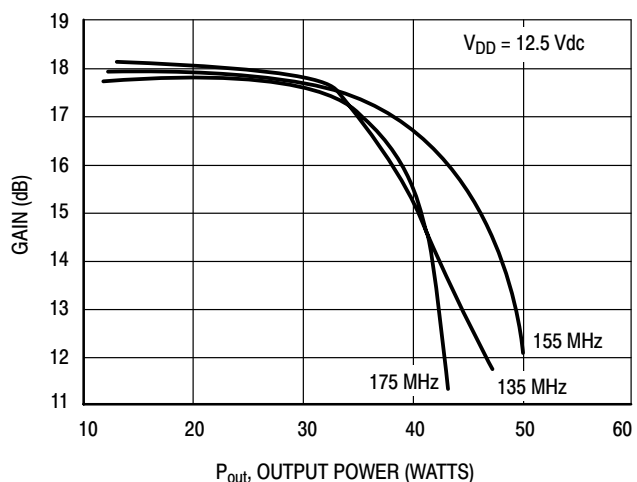


Figure 4. Gain versus Output Power

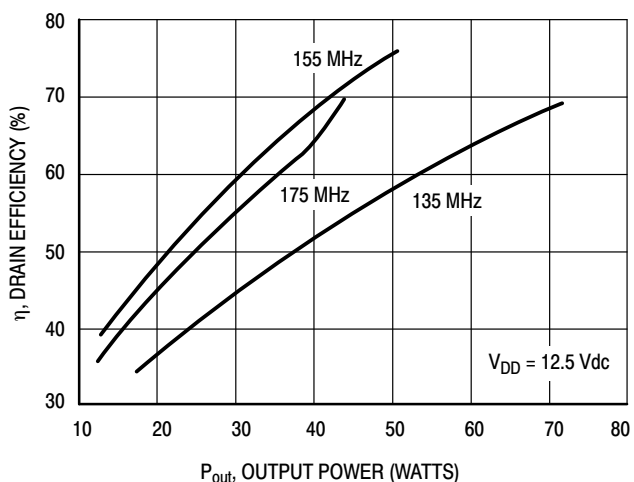


Figure 5. Drain Efficiency versus Output Power

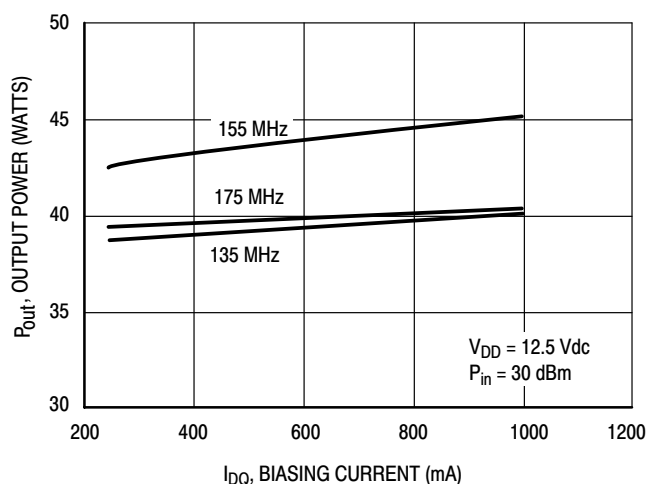


Figure 6. Output Power versus Biasing Current

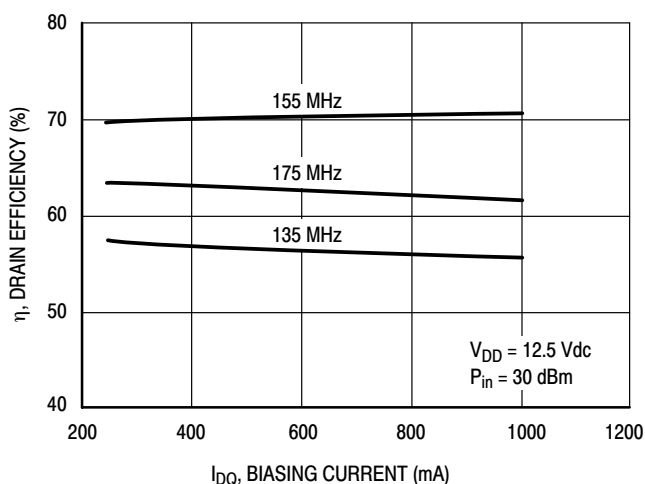


Figure 7. Drain Efficiency versus Biasing Current

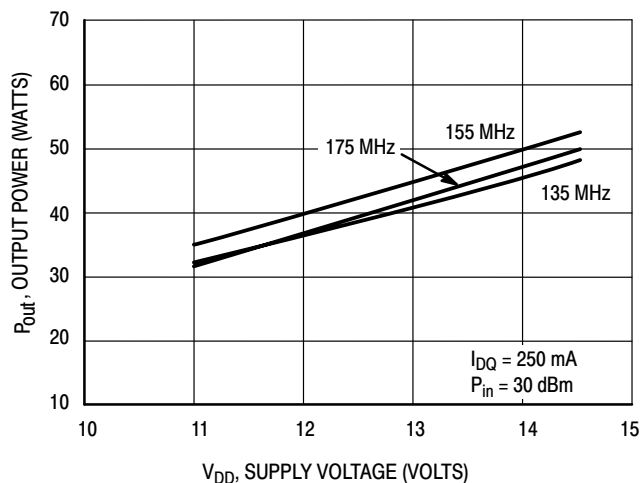


Figure 8. Output Power versus Supply Voltage

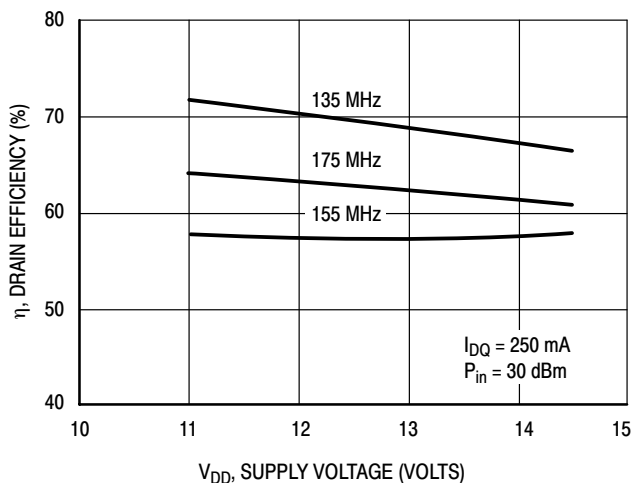
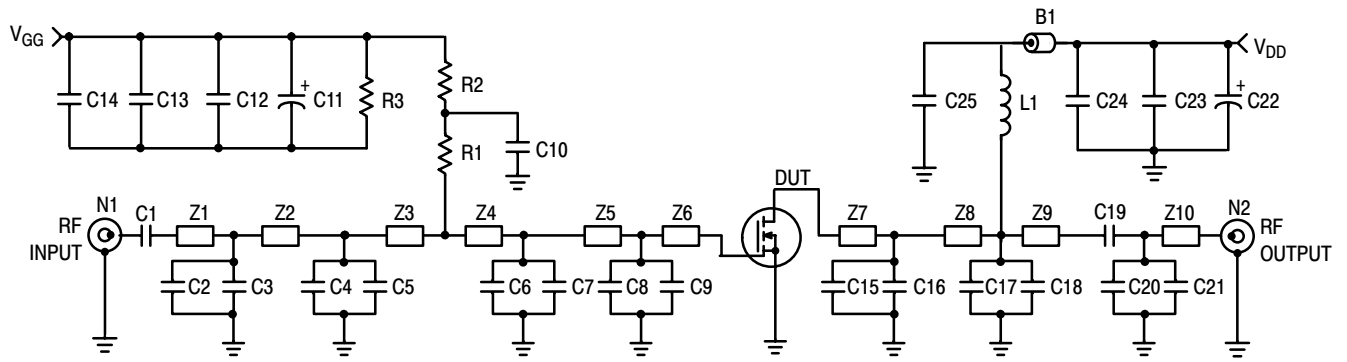


Figure 9. Drain Efficiency versus Supply Voltage



B1	Ferroxcube VK200	C21	1.8 pF, 100 mil Chip Capacitor
C1	160 pF, 100 mil Chip Capacitor	L1	47.5 nH, 5 Turn, Coilcraft
C2	3 pF, 100 mil Chip Capacitor	N1, N2	Type N Flange Mounts
C3	3.6 pF, 100 mil Chip Capacitor	R1	500 Ω Chip Resistor (0805)
C4	2.2 pF, 100 mil Chip Capacitor	R2	1 k Ω Chip Resistor (0805)
C5	10 pF, 100 mil Chip Capacitor	R3	33 k Ω , 1/8 W Chip Resistor
C6, C7	16 pF, 100 mil Chip Capacitors	Z1	0.480" x 0.080" Microstrip
C8, C15, C16	27 pF, 100 mil Chip Capacitors	Z2	1.070" x 0.080" Microstrip
C9	43 pF, 100 mil Chip Capacitor	Z3	0.290" x 0.080" Microstrip
C10, C14, C25	160 pF, 100 mil Chip Capacitors	Z4	0.160" x 0.080" Microstrip
C11, C22	10 μ F, 50 V Electrolytic Capacitors	Z5, Z8	0.120" x 0.080" Microstrip
C12, C24	1,200 pF, 100 mil Chip Capacitors	Z6, Z7	0.120" x 0.223" Microstrip
C13, C23	0.1 μ F, 100 mil Chip Capacitors	Z9	1.380" x 0.080" Microstrip
C17, C18	24 pF, 100 mil Chip Capacitors	Z10	0.625" x 0.080" Microstrip
C19	160 pF, 100 mil Chip Capacitor	Board	Glass Teflon [®] , 31 mils
C20	8.2 pF, 100 mil Chip Capacitor		

Figure 10. 450 - 520 MHz Broadband Test Circuit

TYPICAL CHARACTERISTICS, 450 - 520 MHz

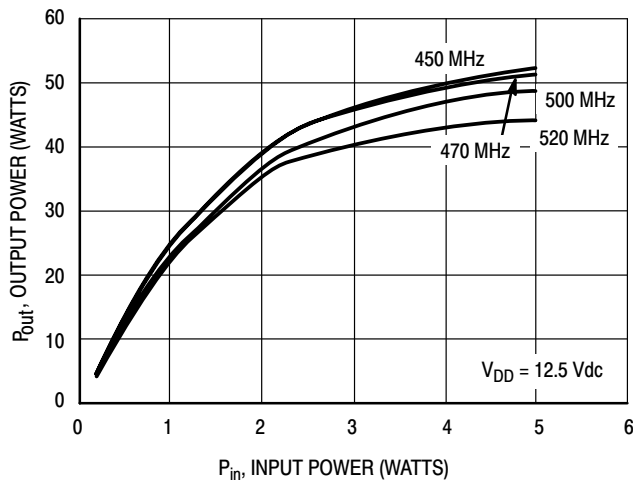


Figure 11. Output Power versus Input Power

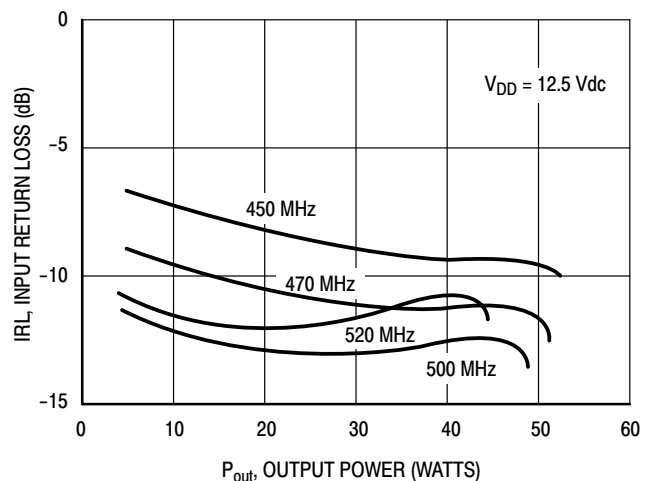


Figure 12. Input Return Loss versus Output Power

TYPICAL CHARACTERISTICS, 450 - 520 MHz

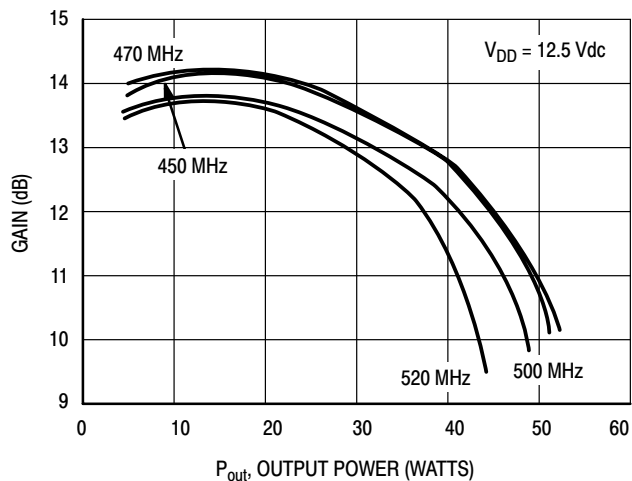


Figure 13. Gain versus Output Power

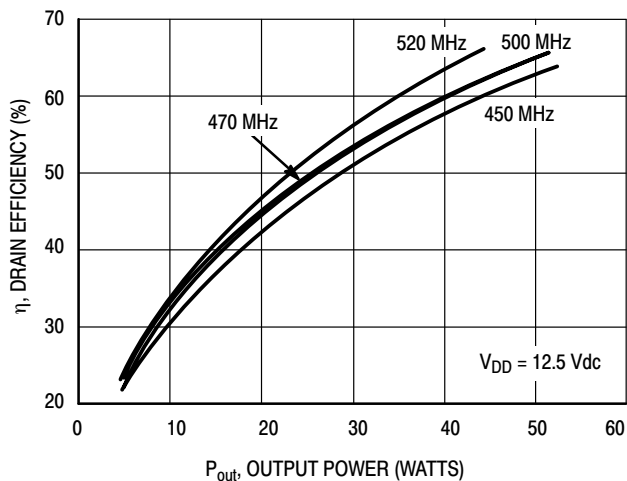


Figure 14. Drain Efficiency versus Output Power

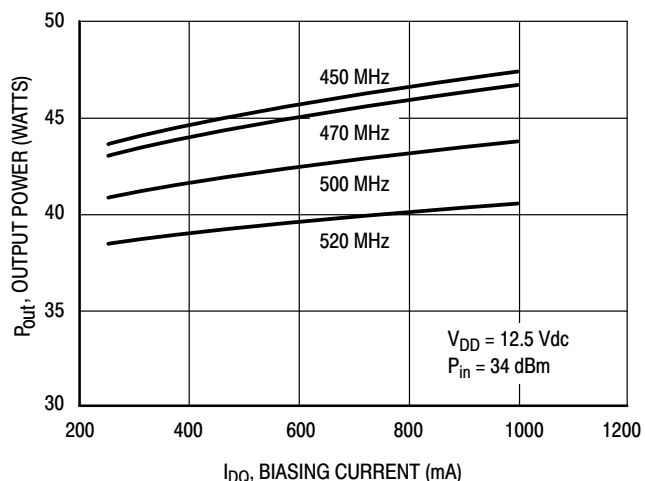


Figure 15. Output Power versus Biasing Current

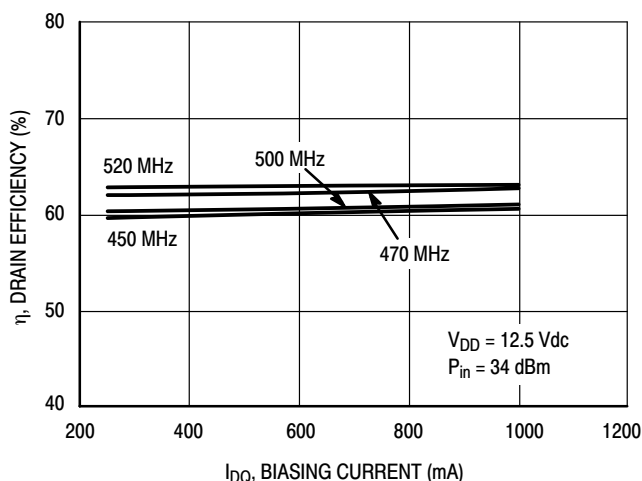


Figure 16. Drain Efficiency versus Biasing Current

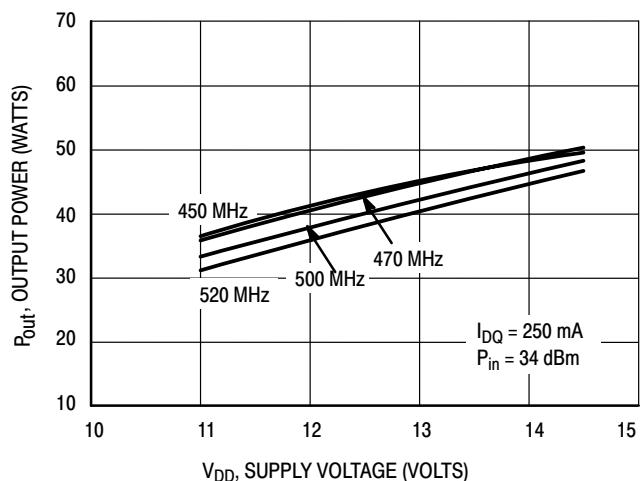


Figure 17. Output Power versus Supply Voltage

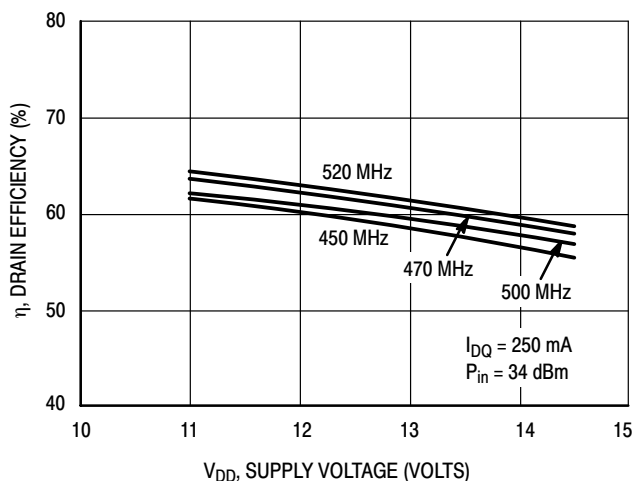
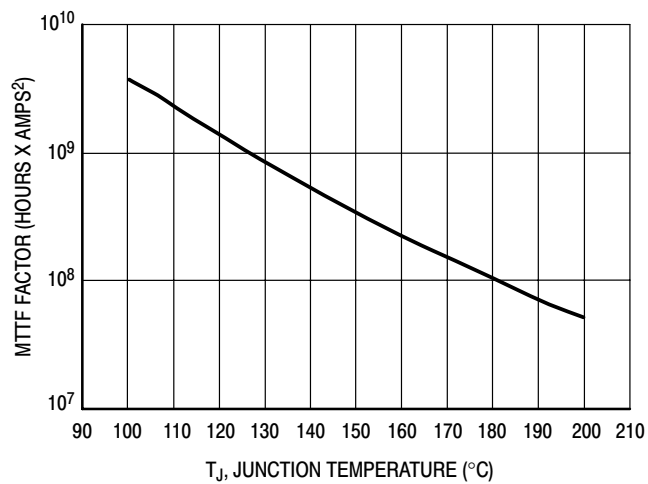


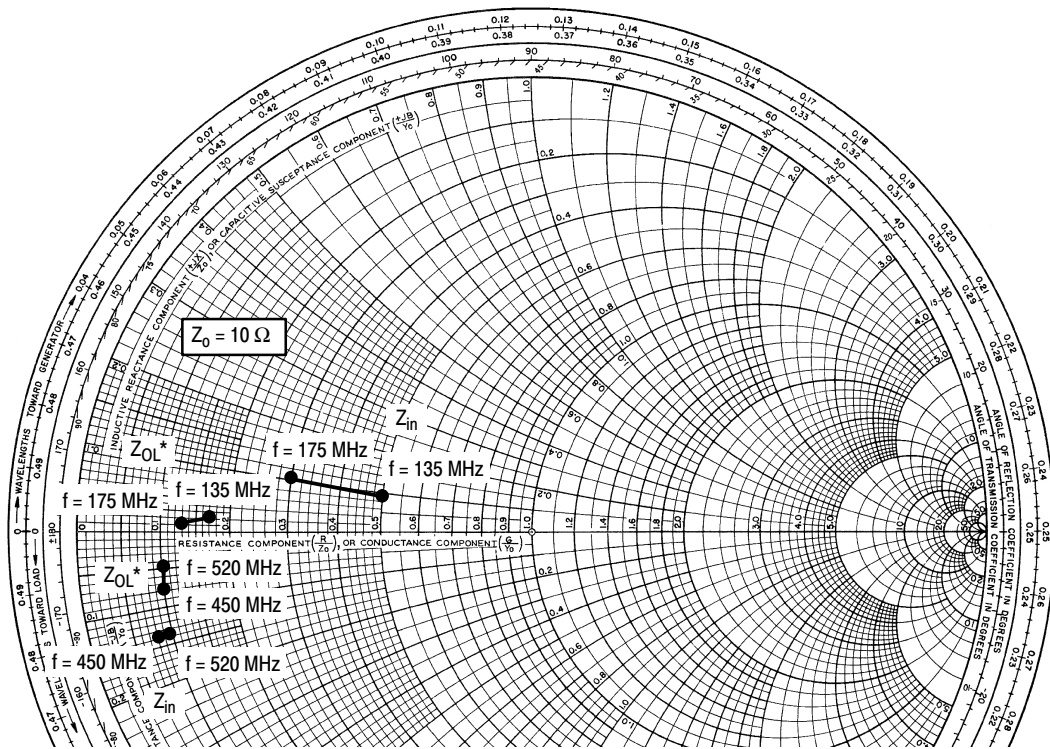
Figure 18. Drain Efficiency versus Supply Voltage

TYPICAL CHARACTERISTICS



This above graph displays calculated MTTF in hours x ampere² drain current. Life tests at elevated temperatures have correlated to better than $\pm 10\%$ of the theoretical prediction for metal failure. Divide MTTF factor by I_D^2 for MTTF in a particular application.

Figure 19. MTTF Factor versus Junction Temperature



$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 250 \text{ mA}$, $P_{out} = 35 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
135	$5.0 + j0.9$	$1.7 + j0.2$
155	$5.0 + j0.9$	$1.7 + j0.2$
175	$3.0 + j1.0$	$1.3 + j0.1$

$V_{DD} = 12.5 \text{ V}$, $I_{DQ} = 500 \text{ mA}$, $P_{out} = 35 \text{ W}$

f MHz	Z_{in} Ω	Z_{OL}^* Ω
450	$0.8 - j1.4$	$1.0 - j0.8$
470	$0.9 - j1.4$	$1.1 - j0.6$
500	$1.0 - j1.4$	$1.1 - j0.6$
520	$0.9 - j1.4$	$1.1 - j0.5$

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50\%$.

Z_{in} = Complex conjugate of source impedance.

Z_{OL}^* = Complex conjugate of the load impedance at given output power, voltage, frequency, and $\eta_D > 50\%$.

Note: Z_{OL}^* was chosen based on tradeoffs between gain, drain efficiency, and device stability.

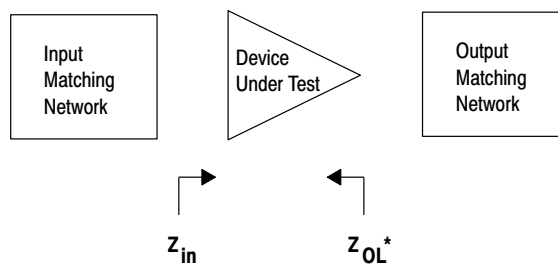


Figure 20. Series Equivalent Input and Output Impedance

Table 5. Common Source Scattering Parameters ($V_{DD} = 12.5 \text{ Vdc}$)

$I_{DQ} = 250 \text{ mA}$

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
50	0.89	-173	8.496	83	0.014	-26	0.76	-170
100	0.90	-175	3.936	72	0.014	-14	0.79	-170
150	0.91	-175	2.429	63	0.011	-23	0.82	-170
200	0.92	-175	1.627	57	0.010	-44	0.86	-170
250	0.94	-176	1.186	53	0.007	-16	0.88	-170
300	0.95	-176	0.888	49	0.005	-44	0.91	-171
350	0.96	-176	0.686	48	0.005	36	0.92	-170
400	0.96	-176	0.568	44	0.005	-1	0.94	-171
450	0.97	-176	0.457	44	0.004	49	0.94	-172
500	0.97	-176	0.394	44	0.003	-51	0.95	-171
550	0.98	-176	0.332	42	0.001	31	0.95	-173
600	0.98	-177	0.286	41	0.013	99	0.94	-173

$I_{DQ} = 1.0 \text{ A}$

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
50	0.90	-173	8.49	83	0.006	-39	0.86	-176
100	0.90	-175	3.92	72	0.009	-5	0.86	-176
150	0.91	-175	2.44	63	0.006	7	0.87	-176
200	0.92	-175	1.62	57	0.008	21	0.88	-175
250	0.94	-176	1.19	53	0.006	8	0.89	-174
300	0.95	-176	0.89	48	0.008	3	0.89	-174
350	0.96	-176	0.69	48	0.007	48	0.91	-174
400	0.96	-176	0.57	44	0.004	41	0.93	-173
450	0.97	-176	0.46	44	0.004	43	0.93	-173
500	0.97	-176	0.39	44	0.003	57	0.94	-173
550	0.98	-176	0.33	41	0.006	62	0.94	-174
600	0.98	-177	0.28	41	0.009	96	0.93	-173

$I_{DQ} = 2.0 \text{ A}$

f MHz	S_{11}		S_{21}		S_{12}		S_{22}	
	$ S_{11} $	$\angle \phi$	$ S_{21} $	$\angle \phi$	$ S_{12} $	$\angle \phi$	$ S_{22} $	$\angle \phi$
50	0.94	-176	9.42	88	0.005	-72	0.89	-177
100	0.94	-178	4.56	82	0.005	4	0.89	-177
150	0.94	-178	2.99	78	0.003	7	0.89	-177
200	0.94	-178	2.14	74	0.005	17	0.90	-176
250	0.95	-178	1.67	71	0.004	40	0.90	-175
300	0.95	-178	1.32	67	0.007	35	0.91	-175
350	0.95	-178	1.08	67	0.005	57	0.92	-174
400	0.96	-178	0.93	63	0.003	50	0.93	-173
450	0.96	-178	0.78	62	0.007	68	0.93	-173
500	0.96	-177	0.68	61	0.004	99	0.94	-173
550	0.97	-177	0.59	58	0.008	78	0.93	-175
600	0.97	-178	0.51	57	0.009	92	0.92	-174

APPLICATIONS INFORMATION

DESIGN CONSIDERATIONS

This device is a common-source, RF power, N-Channel enhancement mode, Lateral Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET). Freescale Application Note AN211A, "FETs in Theory and Practice", is suggested reading for those not familiar with the construction and characteristics of FETs.

This surface mount packaged device was designed primarily for VHF and UHF mobile power amplifier applications. Manufacturability is improved by utilizing the tape and reel capability for fully automated pick and placement of parts. However, care should be taken in the design process to insure proper heat sinking of the device.

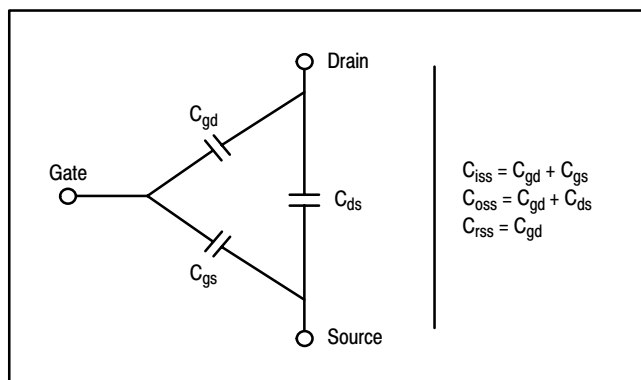
The major advantages of Lateral RF power MOSFETs include high gain, simple bias systems, relative immunity from thermal runaway, and the ability to withstand severely mismatched loads without suffering damage.

MOSFET CAPACITANCES

The physical structure of a MOSFET results in capacitors between all three terminals. The metal oxide gate structure determines the capacitors from gate-to-drain (C_{gd}), and gate-to-source (C_{gs}). The PN junction formed during fabrication of the RF MOSFET results in a junction capacitance from drain-to-source (C_{ds}). These capacitances are characterized as input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances on data sheets. The relationships between the inter-terminal capacitances and those given on data sheets are shown below. The C_{iss} can be specified in two ways:

1. Drain shorted to source and positive voltage at the gate.
2. Positive voltage of the drain in respect to source and zero volts at the gate.

In the latter case, the numbers are lower. However, neither method represents the actual operating conditions in RF applications.



DRAIN CHARACTERISTICS

One critical figure of merit for a FET is its static resistance in the full-on condition. This on-resistance, $R_{DS(on)}$, occurs in the linear region of the output characteristic and is specified at a specific gate-source voltage and drain current. The

drain-source voltage under these conditions is termed $V_{DS(on)}$. For MOSFETs, $V_{DS(on)}$ has a positive temperature coefficient at high temperatures because it contributes to the power dissipation within the device.

BV_{DSS} values for this device are higher than normally required for typical applications. Measurement of BV_{DSS} is not recommended and may result in possible damage to the device.

GATE CHARACTERISTICS

The gate of the RF MOSFET is a polysilicon material, and is electrically isolated from the source by a layer of oxide. The DC input resistance is very high - on the order of $10^9 \Omega$ — resulting in a leakage current of a few nanoamperes.

Gate control is achieved by applying a positive voltage to the gate greater than the gate-to-source threshold voltage, $V_{GS(th)}$.

Gate Voltage Rating — Never exceed the gate voltage rating. Exceeding the rated V_{GS} can result in permanent damage to the oxide layer in the gate region.

Gate Termination — The gates of these devices are essentially capacitors. Circuits that leave the gate open-circuited or floating should be avoided. These conditions can result in turn-on of the devices due to voltage build-up on the input capacitor due to leakage currents or pickup.

Gate Protection — These devices do not have an internal monolithic zener diode from gate-to-source. If gate protection is required, an external zener diode is recommended. Using a resistor to keep the gate-to-source impedance low also helps dampen transients and serves another important function. Voltage transients on the drain can be coupled to the gate through the parasitic gate-drain capacitance. If the gate-to-source impedance and the rate of voltage change on the drain are both high, then the signal coupled to the gate may be large enough to exceed the gate-threshold voltage and turn the device on.

DC BIAS

Since this device is an enhancement mode FET, drain current flows only when the gate is at a higher potential than the source. RF power FETs operate optimally with a quiescent drain current (I_{DQ}), whose value is application dependent. This device was characterized at $I_{DQ} = 500 \text{ mA}$, which is the suggested value of bias current for typical applications. For special applications such as linear amplification, I_{DQ} may have to be selected to optimize the critical parameters.

The gate is a dc open circuit and draws no current. Therefore, the gate bias circuit may generally be just a simple resistive divider network. Some special applications may require a more elaborate bias system.

GAIN CONTROL

Power output of this device may be controlled to some degree with a low power dc control signal applied to the gate, thus facilitating applications such as manual gain control, ALC/AGC and modulation systems. This characteristic is very dependent on frequency and load line.

AMPLIFIER DESIGN

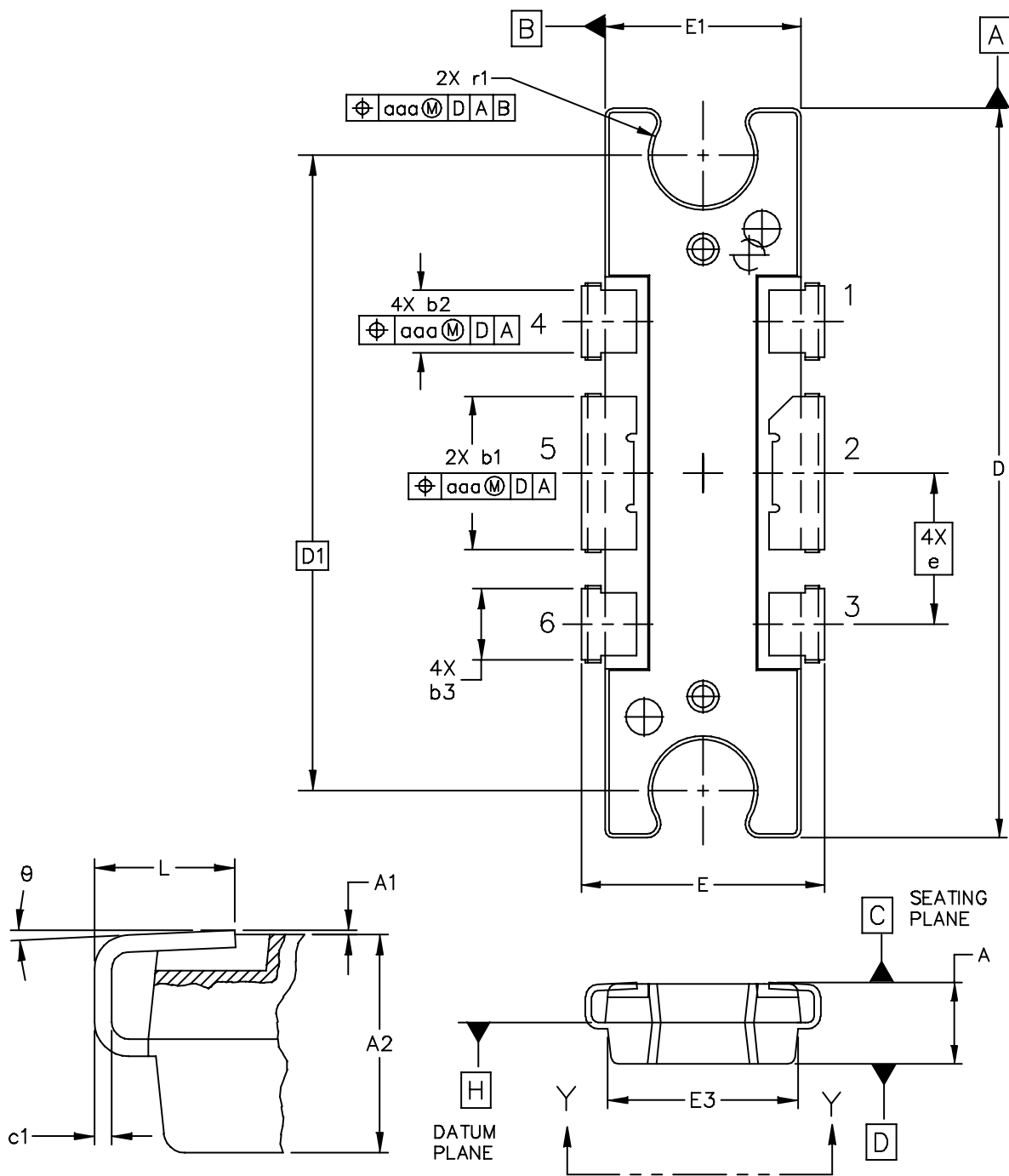
Impedance matching networks similar to those used with bipolar transistors are suitable for this device. For examples see Freescale Application Note AN721, "Impedance Matching Networks Applied to RF Power Transistors." Large-signal impedances are provided, and will yield a good first pass approximation.

Since RF power MOSFETs are triode devices, they are not unilateral. This coupled with the very high gain of this device yields a device capable of self oscillation. Stability may be achieved by techniques such as drain loading, input shunt

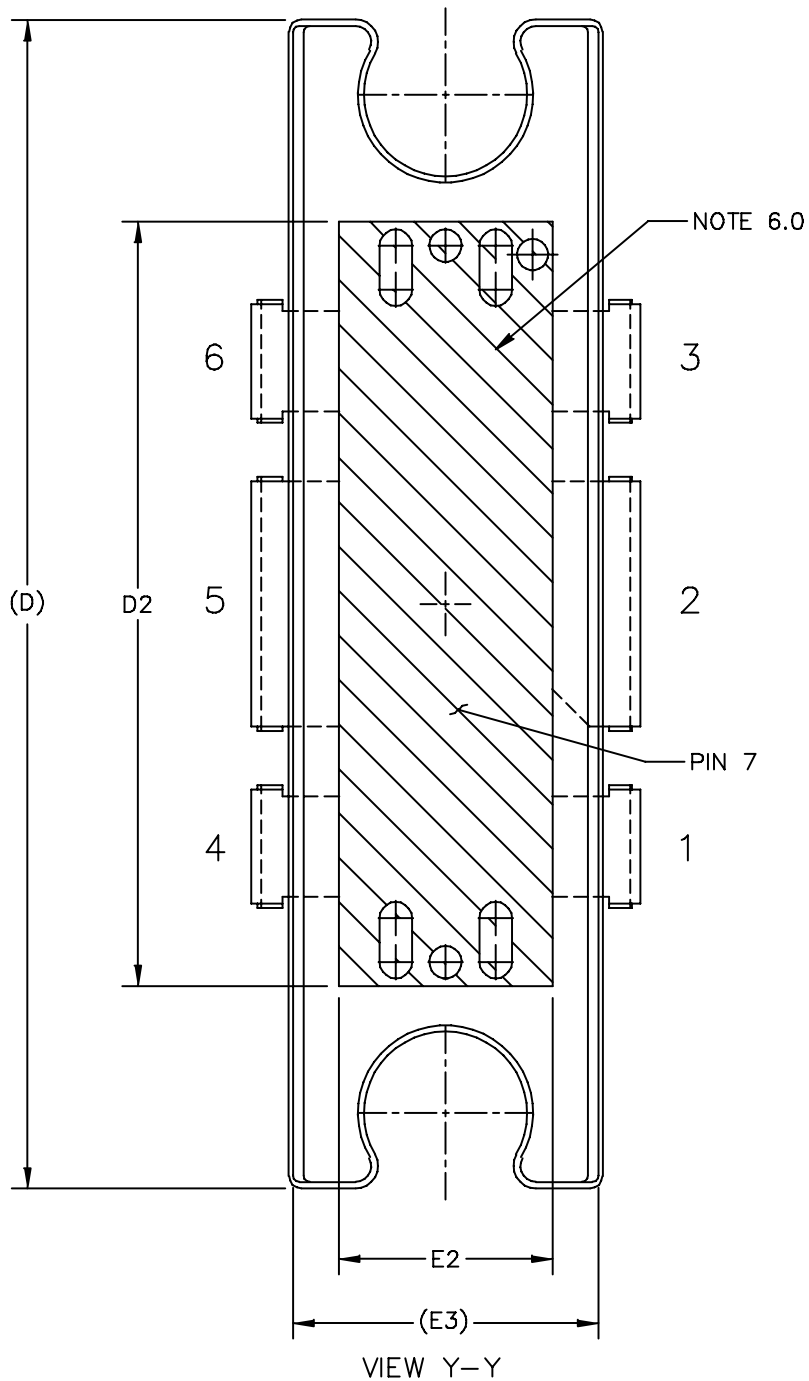
resistive loading, or output to input feedback. The RF test fixture implements a parallel resistor and capacitor in series with the gate, and has a load line selected for a higher efficiency, lower gain, and more stable operating region.

Two-port stability analysis with this device's S-parameters provides a useful tool for selection of loading or feedback circuitry to assure stable operation. See Freescale Application Note AN215A, "RF Small-Signal Design Using Two-Port Parameters" for a discussion of two port network theory and stability.

PACKAGE DIMENSIONS



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TITLE: TO-272 SCREW DOWN MOUNT	DOCUMENT NO: 98ASH98116A	REV: L	
	CASE NUMBER: 1264-10	03 AUG 2007	
	STANDARD: JEDEC TO-272 AA		



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	STANDARD: JEDEC TO-272 AA		

NOTES:

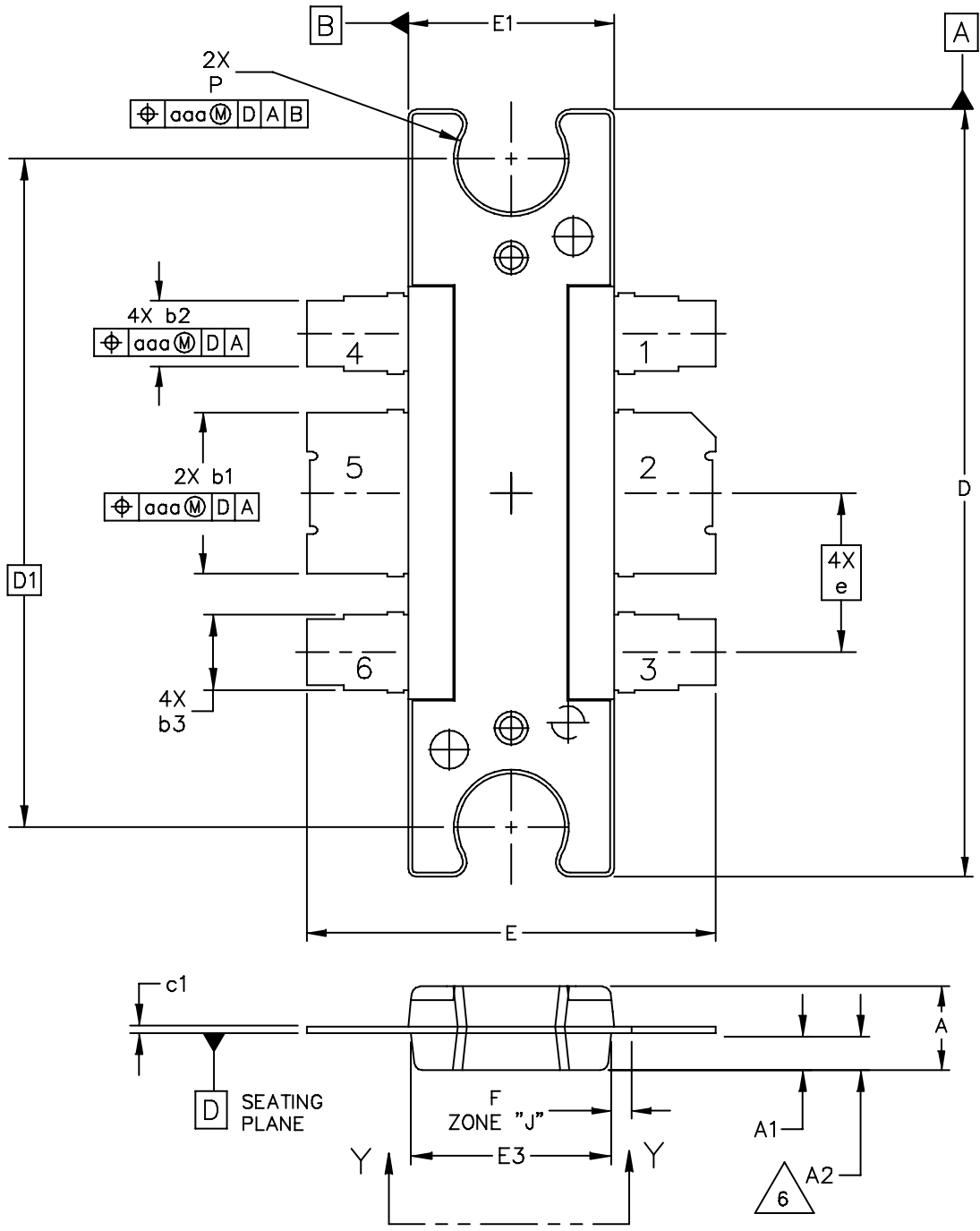
1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DATUM PLANE -H- IS LOCATED AT THE TOP OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE TOP OF THE PARTING LINE.
4. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS "b1" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" AND "b2" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
6. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.

STYLE 1:

PIN 1 - SOURCE (COMMON)	PIN 4 - SOURCE (COMMON)
PIN 2 - DRAIN	PIN 5 - GATE
PIN 3 - SOURCE (COMMON)	PIN 6 - SOURCE (COMMON)
	PIN 7 - SOURCE (COMMON)

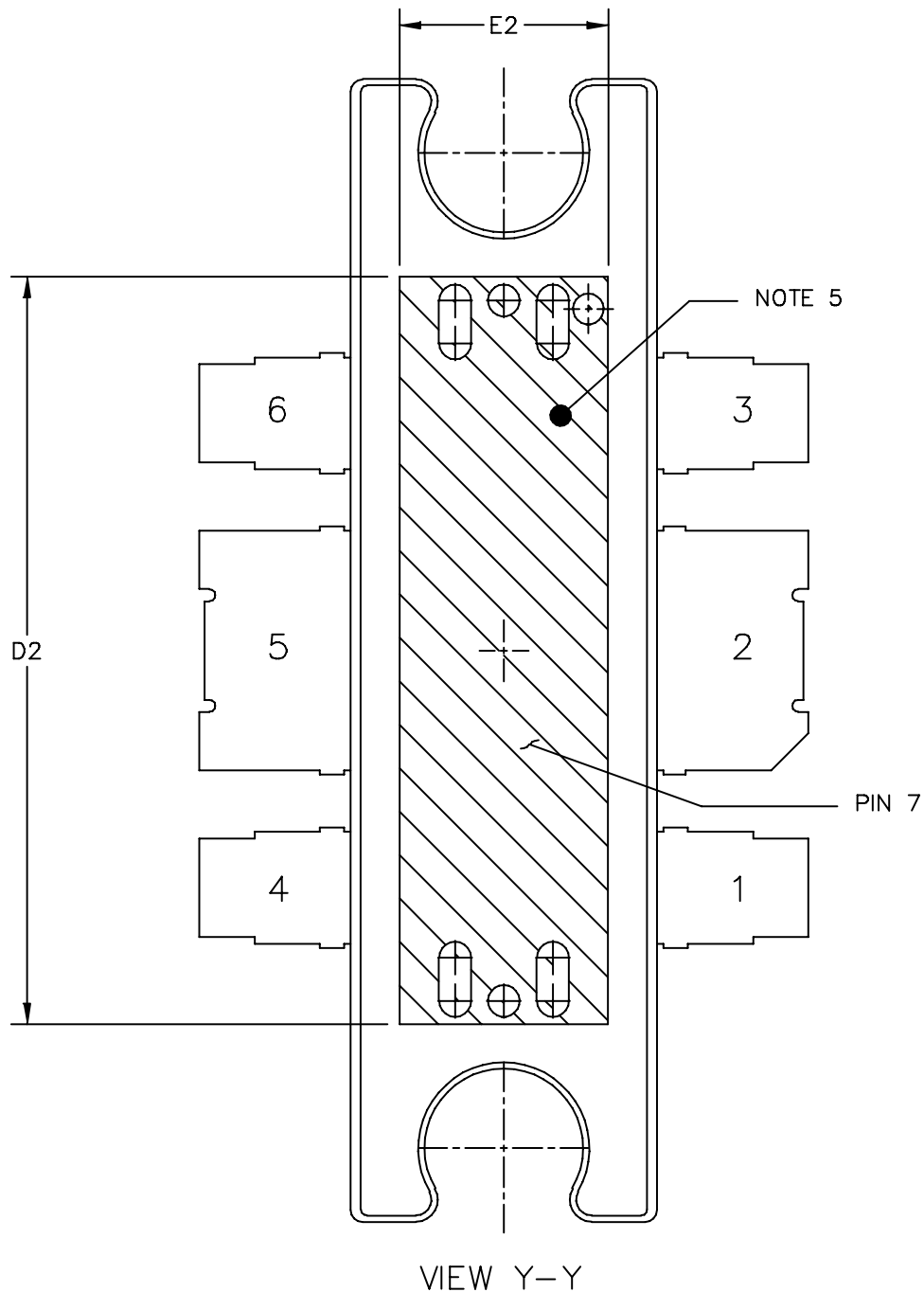
DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.098	.108	2.49	2.74	b1	.193	.199	4.90	5.05
A1	.000	.004	0.00	0.10	b2	.078	.084	1.98	2.13
A2	.100	.104	2.54	2.64	b3	.088	.094	2.24	2.39
D	.928	.932	23.57	23.67	c1	.007	.011	0.18	0.28
D1	.806	.814	20.47	20.68	e	.193 BSC		4.90 BSC	
D2	.604	----	15.34	----	r1	.063	.068	1.60	1.73
E	.296	.304	7.52	7.72	θ	0°	6°	0°	6°
E1	.248	.252	6.30	6.40	aaa	.004		0.1	
E2	.162	----	4.11	----					
E3	.241	.245	6.12	6.22					
L	.060	.070	1.52	1.78					

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TITLE: TO-272, 6 LEAD PLASTIC	DOCUMENT NO: 98ASA10536D		REV: D
	CASE NUMBER: 1264A-03		03 AUG 2007
	STANDARD: JEDEC TO-272 BA		

MRF1535NT1 MRF1535FNT1



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TITLE: TO-272, 6 LEAD PLASTIC	DOCUMENT NO: 98ASA10536D	REV: D	
	CASE NUMBER: 1264A-03	03 AUG 2007	
	STANDARD: JEDEC TO-272 BA		

NOTES:

1. CONTROLLING DIMENSION: INCH
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994.
3. DIMENSIONS "D" AND "E1" DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS .006 PER SIDE. DIMENSIONS "D" AND "E1" DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
4. DIMENSIONS "b1" AND "b3" DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE .005 TOTAL IN EXCESS OF THE "b1" AND "b2" DIMENSIONS AT MAXIMUM MATERIAL CONDITION.
5. CROSSHATCHING REPRESENTS THE EXPOSED AREA OF THE HEAT SLUG.
6. DIMENSION A2 APPLIES WITHIN ZONE "J" ONLY.

STYLE 1:

PIN 1 - SOURCE (COMMON)	PIN 4 - SOURCE (COMMON)
PIN 2 - DRAIN	PIN 5 - GATE
PIN 3 - SOURCE (COMMON)	PIN 6 - SOURCE (COMMON)
	PIN 7 - SOURCE (COMMON)

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.098	.106	2.49	2.69	b1	.193	.199	4.90	5.05
A1	.038	.044	0.96	1.12	b2	.078	.084	1.98	2.13
A2	.040	.042	1.02	1.07	b3	.088	.094	2.24	2.39
D	.926	.934	23.52	23.72	c1	.007	.011	.178	.279
D1	.810 BSC		20.57 BSC		e	.193 BSC		4.90 BSC	
D2	.604	----	15.34	----	aaa	.004		0.1	
E	.492	.500	12.50	12.70					
E1	.246	.254	6.25	6.45					
E2	.162	----	4.11	----					
E3	.241	.245	6.12	6.22					
F	.025 BSC		0.64 BSC						
P	.126	.134	3.20	3.40					

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TITLE: TO-272, 6 LEAD PLASTIC	DOCUMENT NO: 98ASA10536D		REV: D
	CASE NUMBER: 1264A-03		03 AUG 2007
	STANDARD: JEDEC TO-272 BA		

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Application Notes

- AN211A: Field Effect Transistors in Theory and Practice
- AN215A: RF Small-Signal Design Using Two-Port Parameters
- AN721: Impedance Matching Networks Applied to RF Power Transistors
- AN3263: Bolt Down Mounting Method for High Power RF Transistors and RFICs in Over-Molded Plastic Packages

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
11	Feb. 2008	<ul style="list-style-type: none">• Changed DC Bias I_{DQ} value from 150 to 500 to match Functional Test I_{DQ} specification, p. 10• Replaced Case Outline 1264-09 with 1264-10, Issue L, p. 1, 12-14. Removed Drain-ID label from top view and View Y-Y. Corrected cross hatch pattern and its dimensions (D2 and E2) on source contact. Renamed E2 with E3. Added Pin 7 designation. Corrected positional tolerance for bolt hole radius. Added JEDEC Standard Package Number.• Replaced Case Outline 1264A-02 with 1264A-03, Issue D, p. 1, 15-17. Removed Drain-ID label from View Y-Y. Corrected cross hatch pattern and its dimensions (D2 and E2) on source contact (Changed D2 and E2 dimensions from basic to .604 Min and .162 Min, respectively). Added dimension E3. Added Pin 7 designation. Corrected positional tolerance for bolt hole radius. Added JEDEC Standard Package Number.• Added Product Documentation and Revision History, p. 18
12	June 2008	<ul style="list-style-type: none">• Corrected specified performance values for power gain and efficiency on p. 1 to match typical performance values in the functional test table on p. 2

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