



# STP1806

## N-CHANNEL 60V - 0.015 Ω - 50A TO-220 STripFET™ POWER MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP1806	60 V	< 0.018 Ω	50 A

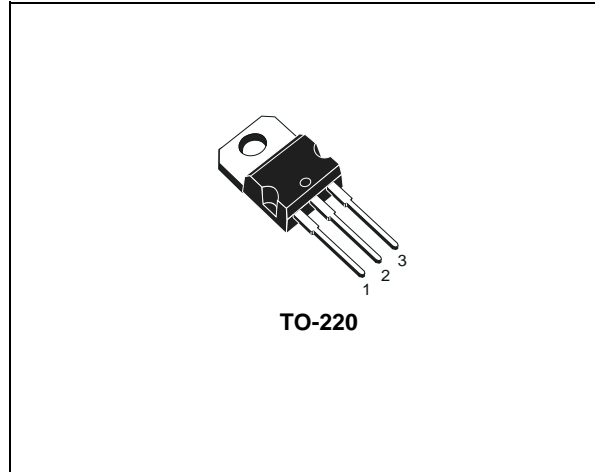
- TYPICAL R<sub>DS(on)</sub> = 0.015 Ω
- EXCEPTIONAL dv/dt CAPABILITY
- 100% AVALANCHE TESTED

### DESCRIPTION

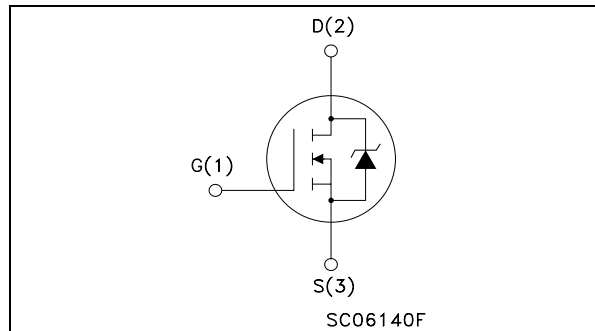
This Power MOSFET is the latest development of STMicroelectronics unique "Single Feature Size™" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

### APPLICATIONS

- HIGH CURRENT, HIGH SWITCHING SPEED
- MOTOR CONTROL
- DC-DC & DC-AC CONVERTERS
- AUTOMOTIVE



### INTERNAL SCHEMATIC DIAGRAM



### Ordering Information

SALES TYPE	MARKING	PACKAGE	PACKAGING
STP1806	P1806	TO-220	TUBE

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	60	V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	60	V
V <sub>GS</sub>	Gate- source Voltage	± 20	V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	50	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	35	A
I <sub>DM</sub> (●)	Drain Current (pulsed)	200	A
P <sub>tot</sub>	Total Dissipation at T <sub>C</sub> = 25°C	110	W
	Derating Factor	0.73	W/°C
dv/dt (1)	Peak Diode Recovery voltage slope	7	V/ns
E <sub>AS</sub> (2)	Single Pulse Avalanche Energy	350	mJ
T <sub>stg</sub>	Storage Temperature	-55 to 175	°C
T <sub>j</sub>	Max. Operating Junction Temperature		

(●) Pulse width limited by safe operating area.

(1) I<sub>SD</sub> ≤ 50A, di/dt ≤ 400A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>, T<sub>j</sub> ≤ T<sub>JMAX</sub>  
 (2) Starting T<sub>j</sub> = 25 °C, I<sub>D</sub> = 25A, V<sub>DD</sub> = 30V

**STP1806****THERMAL DATA**

Rthj-case	Thermal Resistance Junction-case	Max	1.36	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5	°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose		300	°C

**ELECTRICAL CHARACTERISTICS (T<sub>case</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)**

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	60			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ± 20 V			±100	nA

ON (\*)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> I <sub>D</sub> = 250 μA	2	3	4	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10 V I <sub>D</sub> = 27.5 A		0.015	0.018	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (*)	Forward Transconductance	V <sub>DS</sub> = 15 V I <sub>D</sub> = 27.5 A		18		S
C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		1530		pF
C <sub>oss</sub>	Output Capacitance			300		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			105		pF

**ELECTRICAL CHARACTERISTICS** (continued)

**SWITCHING ON**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on Delay Time Rise Time	$V_{DD} = 30\text{ V}$ $I_D = 27.5\text{ A}$ $R_G = 4.7\ \Omega$ $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		16 8		ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 48\text{ V}$ $I_D = 55\text{ A}$ $V_{GS} = 10\text{ V}$		44.5 10.5 17.5	60	nC nC nC

**SWITCHING OFF**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(off)}$ $t_f$	Turn-off Delay Time Fall Time	$V_{DD} = 30\text{ V}$ $I_D = 27.5\text{ A}$ $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (Resistive Load, Figure 3)		36 15		ns ns

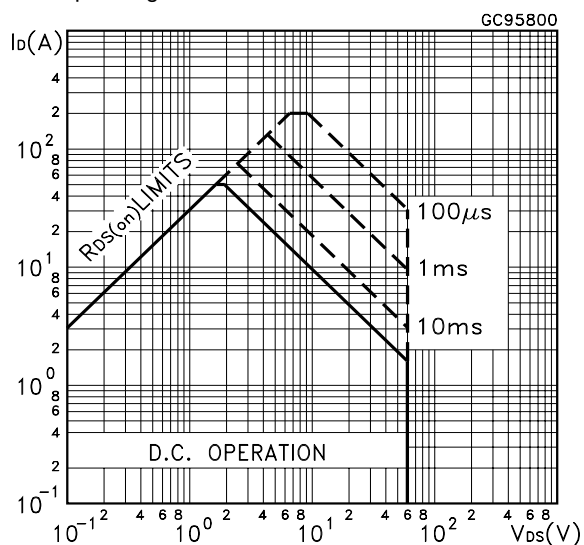
**SOURCE DRAIN DIODE**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (\bullet)$	Source-drain Current Source-drain Current (pulsed)				50 200	A A
$V_{SD} (*)$	Forward On Voltage	$I_{SD} = 55\text{ A}$ $V_{GS} = 0$			1.5	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 55\text{ A}$ $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 30\text{ V}$ $T_j = 150^\circ\text{C}$ (see test circuit, Figure 5)		75 170 4.5		ns nC A

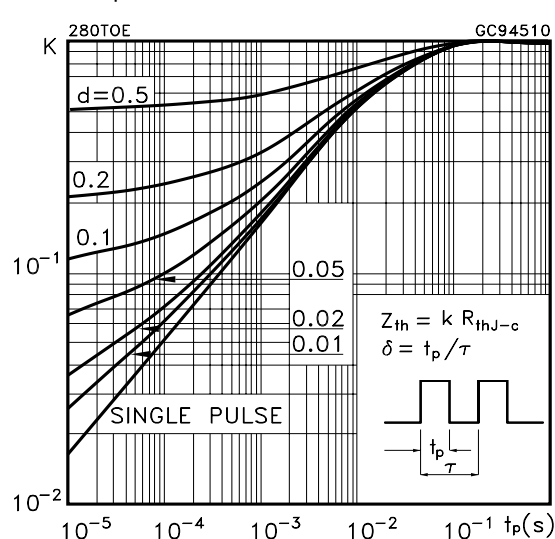
(\*) Pulse width  $\geq 300\ \mu\text{s}$ , duty cycle 1.5 %.

(•) Pulse width limited by safe operating area

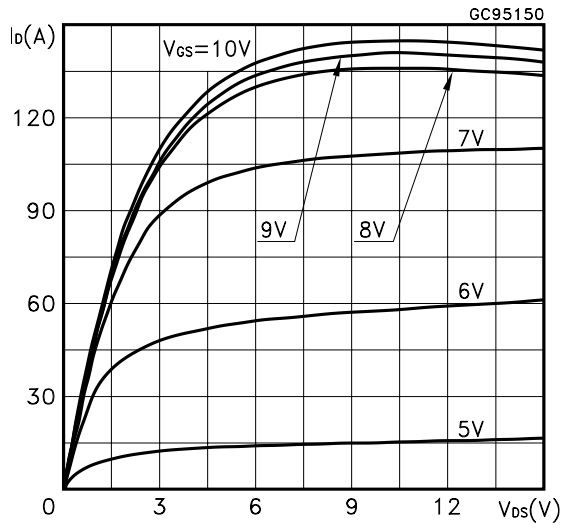
Safe Operating Area



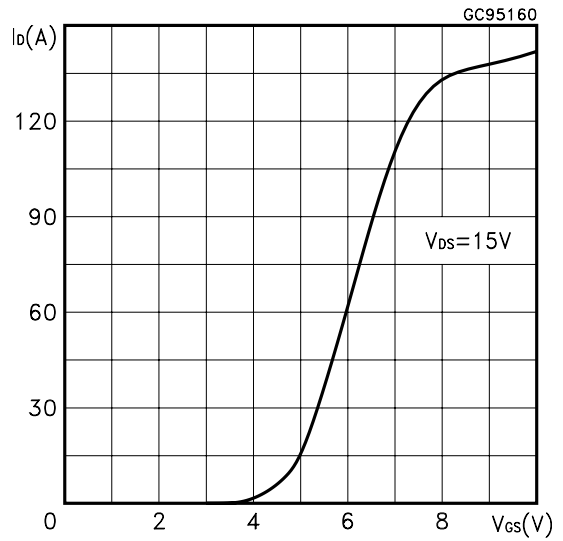
Thermal Impedance



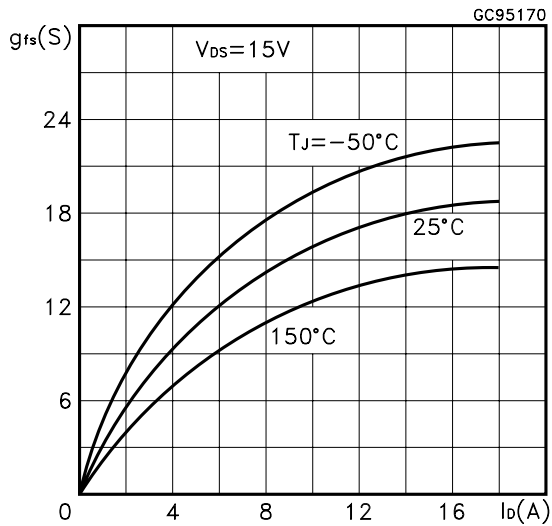
Output Characteristics



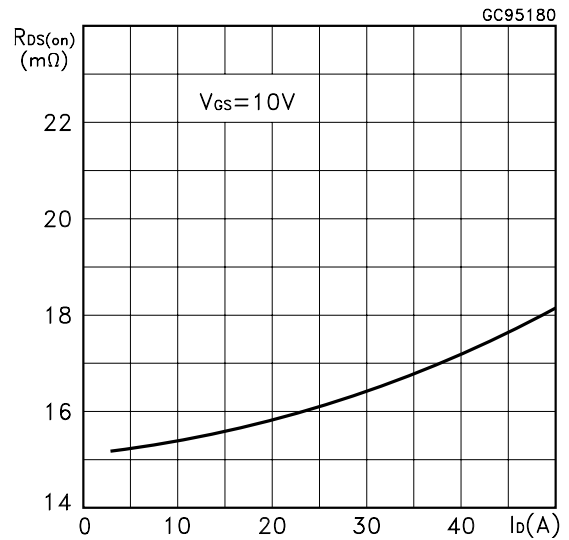
Transfer Characteristics



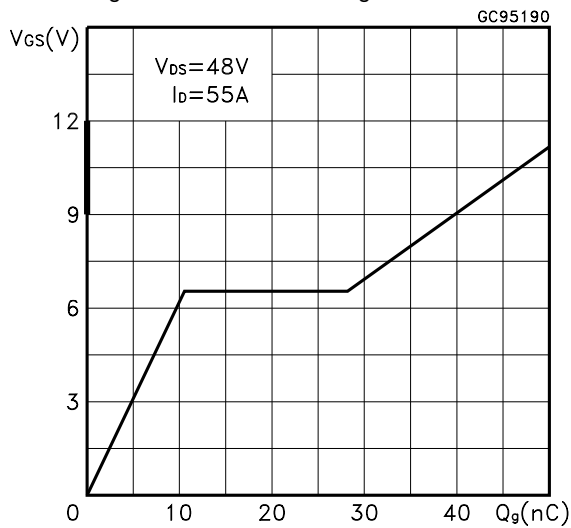
Transconductance



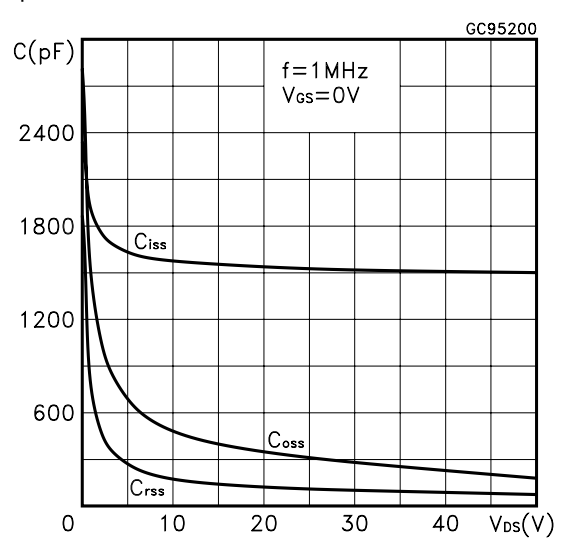
Static Drain-source On Resistance



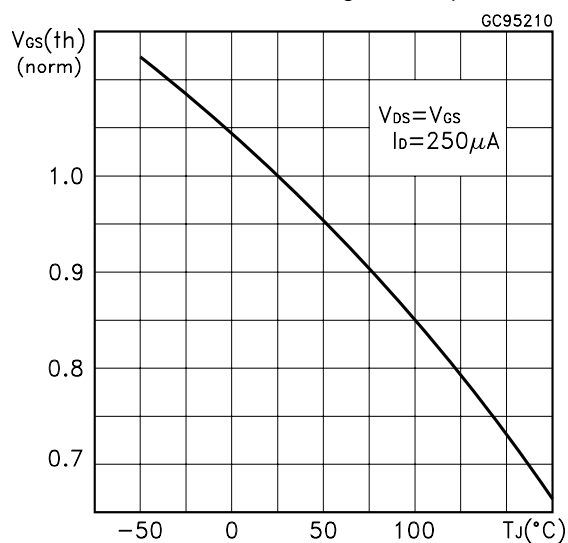
Gate Charge vs Gate-source Voltage



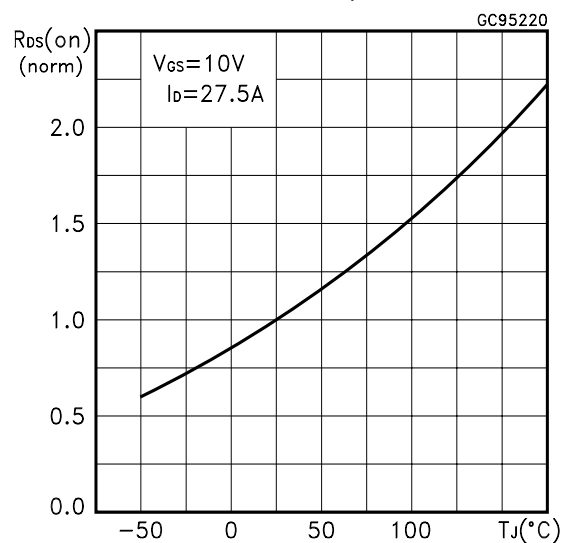
Capacitance Variations



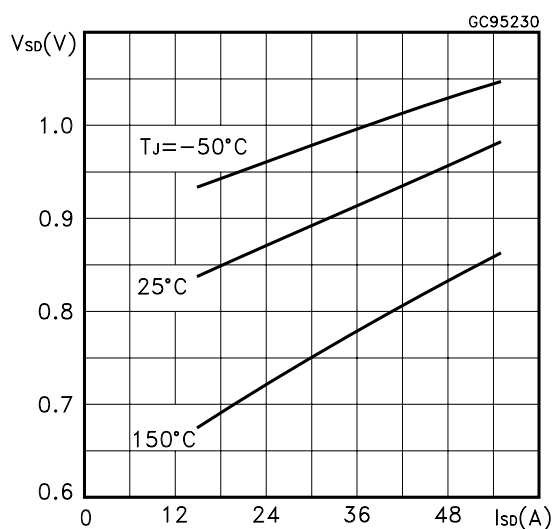
Normalized Gate Threshold Voltage vs Temperature



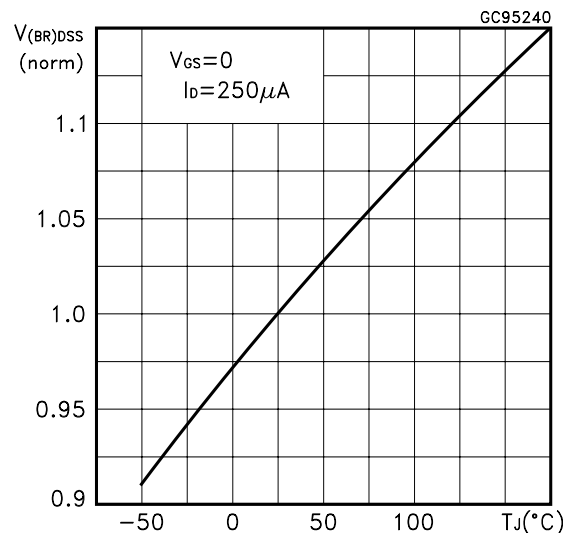
Normalized on Resistance vs Temperature



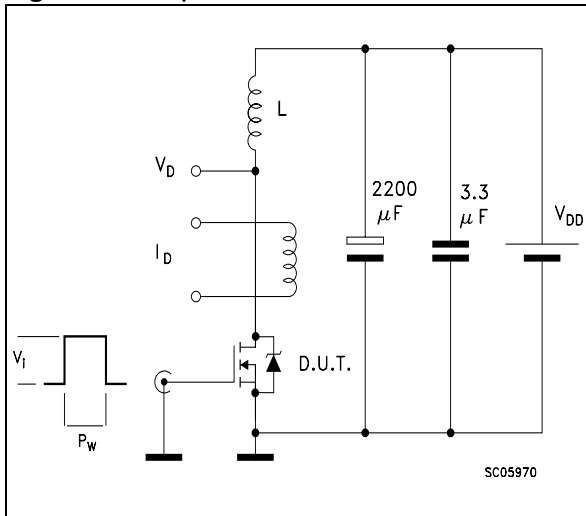
Source-drain Diode Forward Characteristics



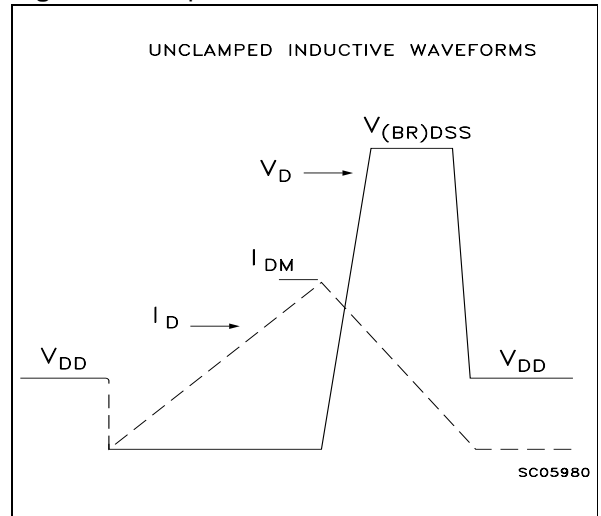
Normalized Breakdown Voltage vs Temperature.



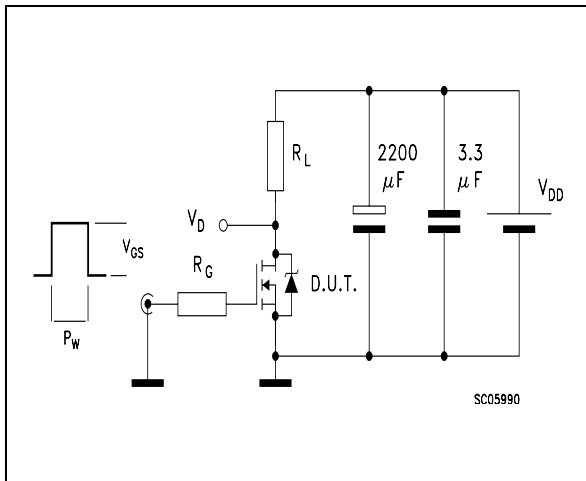
**Fig. 1: Unclamped Inductive Load Test Circuit**



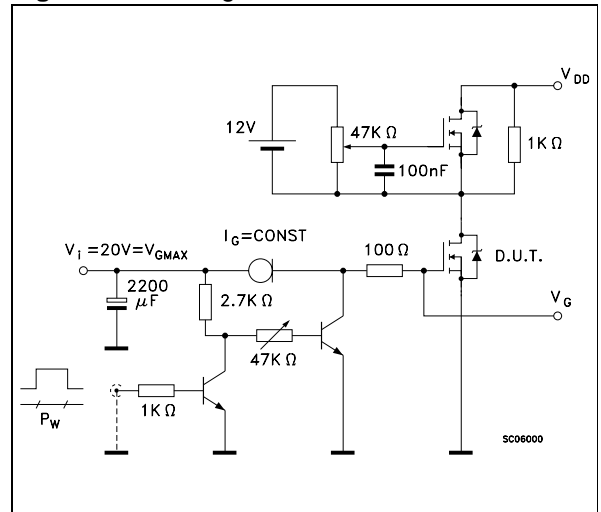
**Fig. 2: Unclamped Inductive Waveform**



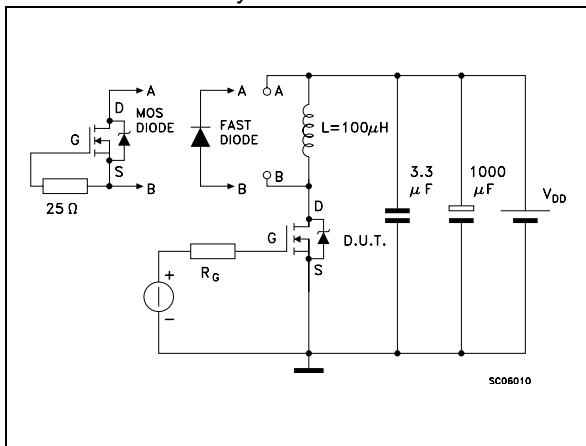
**Fig. 3: Switching Times Test Circuits For Resistive Load**



**Fig. 4: Gate Charge test Circuit**

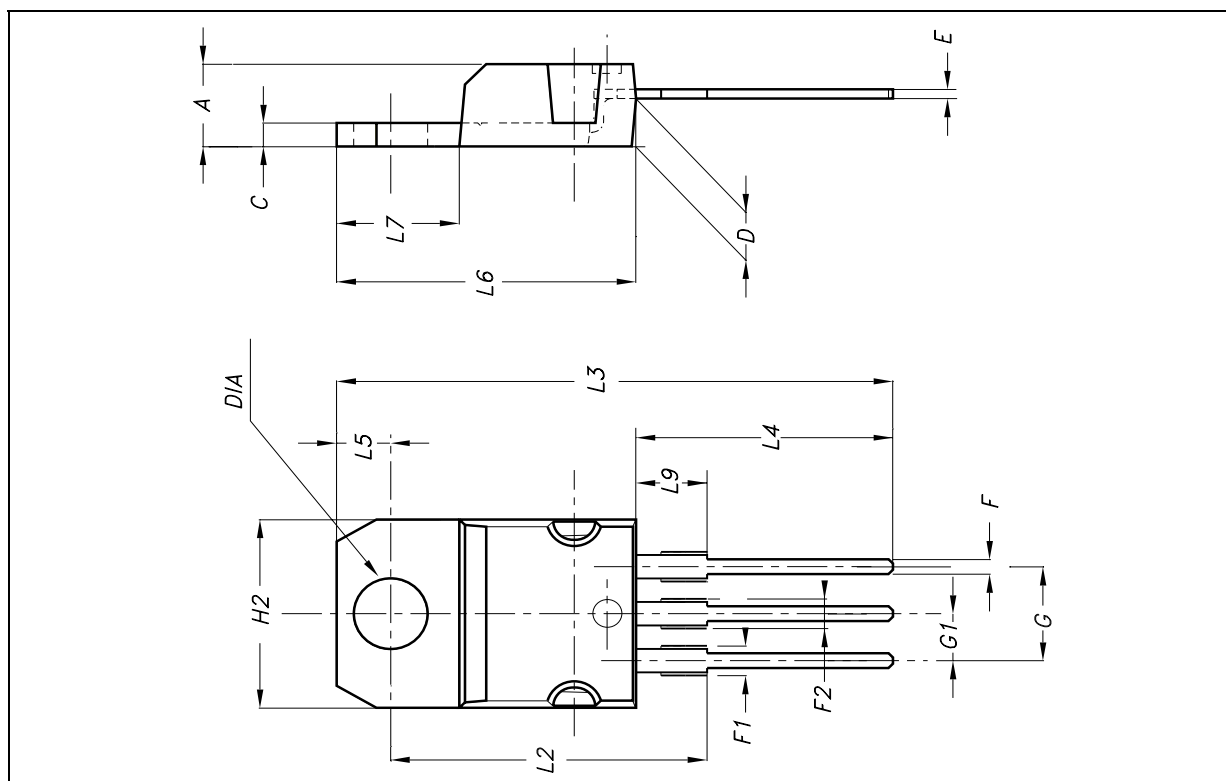


**Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times**



## TO-220 MECHANICAL DATA

DIM.	mm.			inch.		
	MIN.	TYP.	MAX.	MIN.	TYP.	TYP.
A	4.4		4.6	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.40		2.70	0.094		0.106
H2	10		10.40	0.393		0.409
L2		16.40			0.645	
L3		28.90			1.137	
L4	13		14	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.20		6.60	0.244		0.260
L9	3.50		3.93	0.137		0.154
DIA	3.75		3.85	0.147		0.151



### Revision History

Date	Revision	Description of Changes
Tuesday 16 November 2004	0.2	updating marking



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