

Vishay Siliconix

N-Channel 100 V (D-S) 175 °C MOSFET

PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)		
100	0.0095 at V _{GS} = 10 V	110 ^a		

FEATURES

- TrenchFET[®] Power MOSFET
- New Package with Low Thermal Resistance
- 100 % R_g Tested





GDS Top View GO

D 0

Ordering Information: SUM110N10-09-E3 (Lead (Pb)-free)

N-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS $T_{C} = 25 \text{ °C}$, unless otherwise noted						
Parameter	Symbol	Limit	Unit			
Drain-Source Voltage	V _{DS}	100	v			
Gate-Source Voltage	V _{GS}	± 20	v			
Continuous Drain Current ($T_{I} = 175 ^{\circ}C$)	T _C = 25 °C	1	110 ^a			
Continuous Drain Current (1) = 175 C)	T _C = 125 °C	I _D	87 ^a	A		
Pulsed Drain Current	I _{DM}	440	~			
Avalanche Current	I _{AR}	75				
Repetitive Avalanche Energy ^b	L = 0.1 mH	E _{AR}	280	mJ		
Maximum Power Dissipation ^b	T _C = 25 °C	Р	375 ^c	w		
	T _A = 25 °C		3.75	v		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 175	°C		

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Limit	Unit		
Junction-to-Ambient	PCB Mount (TO-263) ^d	R _{thJA}	40	°C/W		
Junction-to-Case (Drain)		R _{thJC}	0.4	0/11		

Notes:

a. Package limited.

b. Duty cycle \leq 1 %.

c. See SOA curve for voltage derating.d. When mounted on 1" square PCB (FR-4 material).

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS} V _{DS} = 0 V, I _D = 250 μA 100		100			V	
Gate-Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \ \mu A$	2		4	V	
Gate-Body Leakage	I _{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA	
		$V_{DS} = 100 \text{ V}, V_{GS} = 0 \text{ V}$			1		
Zero Gate Voltage Drain Current	I _{DSS}	V_{DS} = 100 V, V_{GS} = 0 V, T_{J} = 125 °C			50	μΑ	
		V_{DS} = 100 V, V_{GS} = 0 V, T_{J} = 175 °C			250		
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, \text{ V}_{GS} = 10 \text{ V}$	120			А	
		V _{GS} = 10 V, I _D = 30 A		0.0078	0.0095		
Drain-Source On-State Resistance ^a	R _{DS(on)}	V_{GS} = 10 V, I _D = 30 A, T _J = 125 °C			0.017	Ω	
		V_{GS} = 10 V, I _D = 30 A, T _J = 175 °C			0.025		
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 30 A	25			S	
Dynamic ^b							
Input Capacitance	C _{iss}			6700		pF	
Output Capacitance	C _{oss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		750			
Reverse Transfer Capacitance	C _{rss}			280			
Total Gate Charge ^c	Qg			110	160	nC	
Gate-Source Charge ^c	Q _{gs}	$V_{DS} = 50 \text{ V}, \text{ V}_{GS} = 10 \text{ V}, \text{ I}_{D} = 85 \text{ A}$		24			
Gate-Drain Charge ^c	Q _{gd}			24			
Gate Resistance	Rg		1.0		6.2	Ω	
Turn-On Delay Time ^c	t _{d(on)}			20	30		
Rise Time ^c	t _r	V_{DD} = 50 V, R_{L} = 0.6 Ω		125	200		
Turn-Off Delay Time ^c	t _{d(off)}	$I_D \cong 85 \text{ Å}, V_{GEN} = 10 \text{ V}, R_g = 2.5 \Omega$		55	85	ns	
Fall Time ^c	t _f			130	195		
Source-Drain Diode Ratings and Cha	aracteristics	$\Gamma_{\rm C} = 25 \ ^{\circ}{\rm C}^{\rm b}$			· ·		
Continuous Current	۱ _S				110	^	
Pulsed Current	I _{SM}				240	A	
Forward Voltage ^a	V _{SD}	$I_{F} = 85 \text{ A}, V_{GS} = 0 \text{ V}$		1.0	1.5	V	
Reverse Recovery Time	t _{rr}			70	140	ns	
Peak Reverse Recovery Charge	I _{RM(REC)}	I _F = 50 A, dl/dt = 100 A/μs		5.5	10	Α	
Reverse Recovery Charge	Q _{rr}			0.19	0.35	μC	

Notes:

a. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

b. Guaranteed by design, not subject to production testing.

c. Independent of operating temperature.

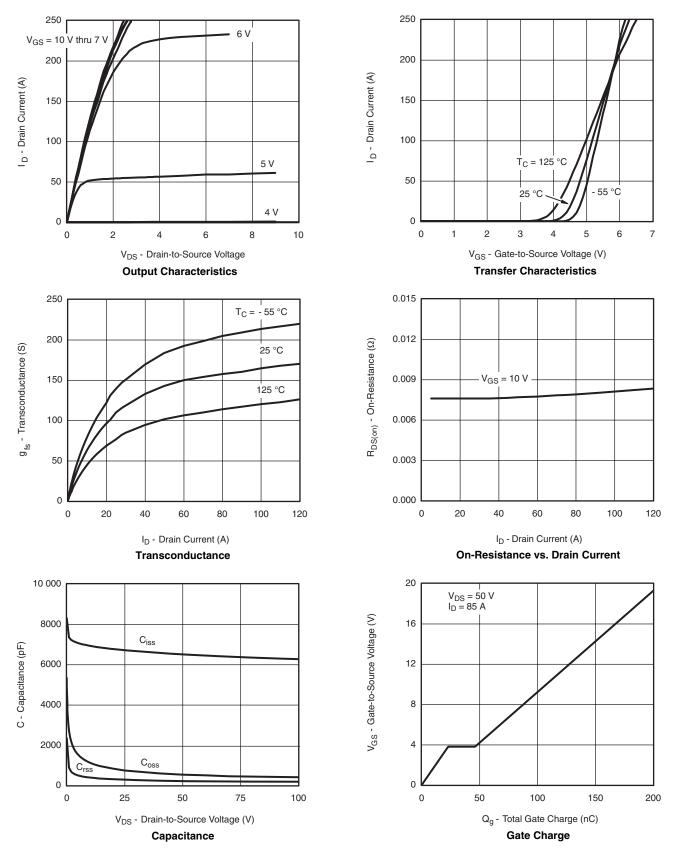
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

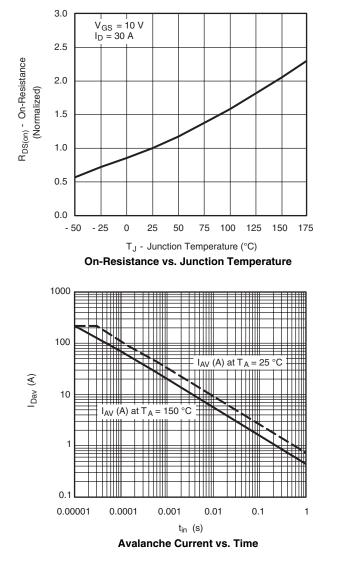


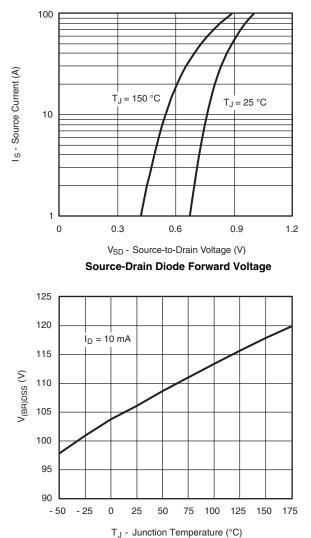
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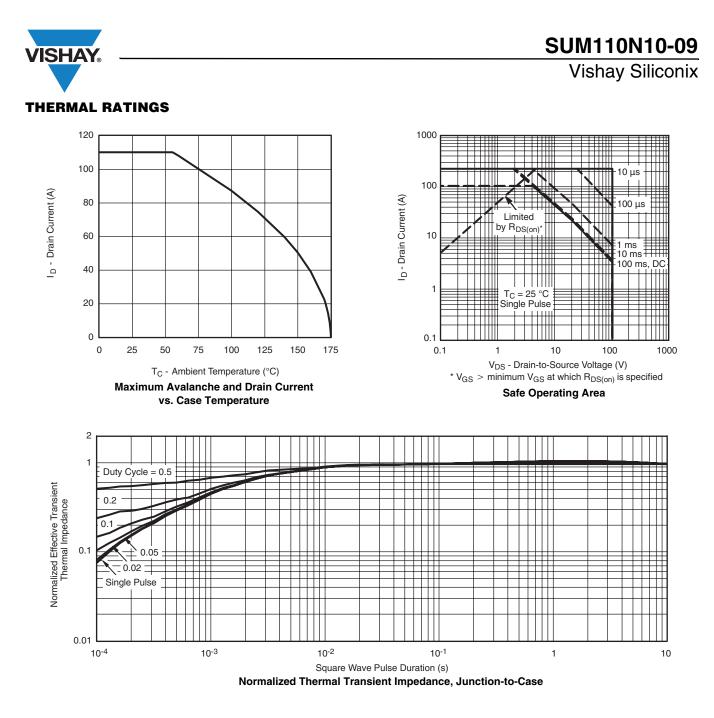


TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted





Drain Source Breakdown vs. Junction Temperature



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <u>www.vishay.com/ppg270677</u>.



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TO-263 (D²PAK): 3-LEAD









DETAIL A (ROTATED 90°)



		INCHES		MILLIMETERS		
DIM.		MIN.	MAX.	MIN.	MAX.	
А		0.160	0.190	4.064	4.826	
b		0.020	0.039	0.508	0.990	
	b1	0.020	0.035	0.508	0.889	
	b2	0.045	0.055	1.143	1.397	
с*	Thin lead	0.013	0.018	0.330	0.457	
C	Thick lead	0.023	0.028	0.584	0.711	
c1	Thin lead	0.013	0.017	0.330	0.431	
CI	Thick lead	0.023	0.027	0.584	0.685	
	c2	0.045	0.055	1.143	1.397	
	D	0.340	0.380	8.636	9.652	
	D1	0.220	0.240	5.588	6.096	
D2		0.038	0.042	0.965	1.067	
D3		0.045	0.055	1.143	1.397	
D4		0.044	0.052	1.118	1.321	
	E	0.380	0.410	9.652	10.414	
	E1	0.245	-	6.223	-	
	E2	0.355	0.375	9.017	9.525	
	E3	0.072	0.078	1.829	1.981	
	е	0.100	0.100 BSC		BSC	
	К	0.045	0.055	1.143	1.397	
	L	0.575	0.625	14.605	15.875	
	L1	0.090	0.110	2.286	2.794	
L2		0.040	0.055	1.016	1.397	
	L3	0.050	0.070	1.270	1.778	
	L4	0.010 BSC		0.254 BSC		
	М	-	0.002	-	0.050	
ECN: T13-0707-Rev. K, 30-Sep-13 DWG: 5843						

Notes

- 1. Plane B includes maximum features of heat sink tab and plastic. 2. No more than 25 % of L1 can fall above seating plane by
- max. 8 mils.3. Pin-to-pin coplanarity max. 4 mils.
- 4. *: Thin lead is for SUB, SYB.
 - Thick lead is for SUM, SYM, SQM.
- 5. Use inches as the primary measurement.

This feature is for thick lead.

Revison: 30-Sep-13



RECOMMENDED MINIMUM PADS FOR D²PAK: 3-Lead



Recommended Minimum Pads Dimensions in Inches/(mm)

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