SYNC COMBINATION WITH TRANSMITTER IDENTIFICATION AND VERTICAL 625 DIVIDER SYSTEM

GENERAL DESCRIPTION

The TDA3571B is a monolithic integrated circuit for use in colour television receivers with switched-mode driven or self-regulating horizontal time-base circuits. It is designed in combination with the TDA2581 to operate as a matched pair. When supplied with a composite video signal the TDA3571B delivers drive pulses for the TDA2581 and sync pulses for the vertical deflection. The circuit is optimized for a horizontal and vertical frequency ratio of 625. It incorporates the following features:

Features

- Horizontal sync separator (including noise inverter)
- Horizontal phase detector
- Horizontal oscillator (31,25 kHz)
- Sandcastle pulse generator
- Vertical sync pulse separator
- Very stable automatic vertical synchronization due to the 625 divider system, without delay after channel change
- Three voltage level sensor on coincidence detector circuit output
- Video transmitter identification circuit for sound muting and search tuning systems
- Inhibit of vertical sync pulse when no video transmitter is detected

QUICK REFERENCE DATA

Supply voltage				
horizontal (pin 14)	$V_{14\text{-}13}$	typ.	12	V
vertical (pin 18)	$V_{18\text{-}13}$	typ.	12	V
Supply current (pin 14 + pin 18)	V_{14+18}	typ.	52	mA
Sync separator				
input voltage level (peak-to-peak value)	$V_{2\text{-}13(p\text{-}p)}$	0,07 to	1	V
slicing level		typ.	50	%
Output pulse				
horizontal (peak-to-peak value)	$V_{8\text{-}13(p\text{-}p)}$	min.	10	V
vertical sync (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	min.	10	V
burst key (peak-to-peak value)	$V_{15\text{-}13(p\text{-}p)}$	min.	10	V
Video transmitter identification circuit				
Output voltage (pin 10)				
sync pulse present	$V_{10\text{-}13}$	typ.	8	V
no sync pulse	$V_{10\text{-}13}$	max.	1	V
Phase locked loop				
control sensitivity		typ.	2000	Hz/μs
holding range	Δf	typ.	± 1000	Hz
catching range	Δf	typ.	± 900	Hz
Operating ambient temperature range	T_{amb}	−25 to +	65	°C

PACKAGE OUTLINE

18-lead DIL; plastic (SOT-102A).

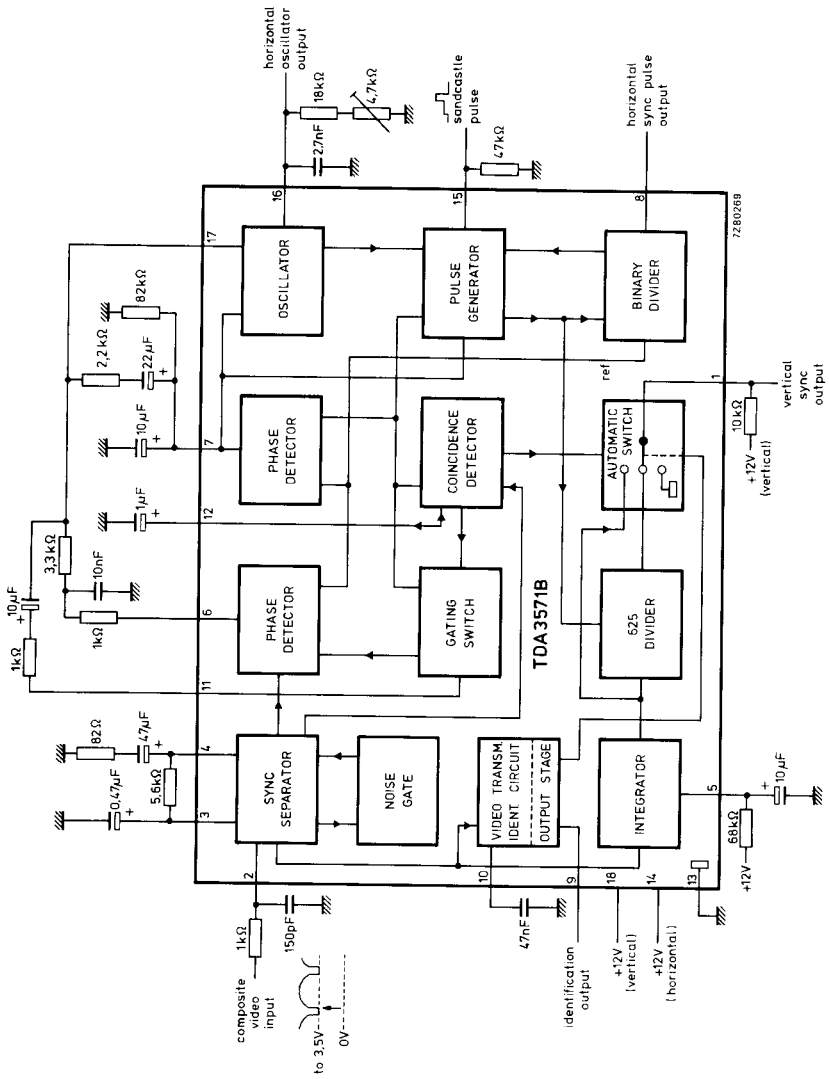

Fig. 1 Block diagram.

FUNCTIONAL DESCRIPTION

The video input voltage to drive the sync separator must have negative-going sync, which can be obtained from synchronous demodulators such as TDA2540, TDA2541 and TDA2670.

The slicing level of the sync separator is determined by the value of the resistor between pins 3 and 4. A 5,6 kΩ resistor provides a slicing level midway between the top sync level and the blanking level. Thus the slicing level is independent of the amplitude of the sync pulse input at pin 2.

The nominal top sync level at pin 2 is 1,5 V, and the amplitude selective noise inverter is activated at 0,7 V. The horizontal phase detector has a steepness of 1,2 V/μs and together with the 1800 Hz/V of the horizontal oscillator provides a total control steepness of 2000 Hz/μs.

A second horizontal phase detector provides a 5,5 μs pulse which ensures symmetrical gating of the horizontal synchronization. During catching the gating is automatically switched off. At the same time the flywheel filter is switched to a short time constant. The value of this time constant can be determined externally via pin 11.

When the indirect vertical sync output is generated by the 625 divider system an anti-top flutter pulse switches off the equalizing and vertical sync pulse operation of the phase detector. Thus top flutter distortion of the control voltage due to vertical pulses can be anticipated. When the 625 divider system is in the direct mode the anti-top flutter pulse is inhibited.

The free running output frequency of the horizontal oscillator is 31,25 kHz. The vertical frequency output is obtained by dividing this double horizontal frequency by 625. The double horizontal frequency is fed via a binary divider to provide the normal 15,625 kHz horizontal output at pin 8. The trailing edge of this pulse is positioned 0,9 μs after the end of the video sync pulse input at pin 2 (see Fig. 2).

The automatic vertical sync block contains the following:

- 625 divider
- In/out-sync detector
- Direct/indirect sync switch
- Identification circuit

It is fed by a signal obtained by integration of the composite sync signal and an internally generated, clipped video signal. The vertical sync pulse is sliced out of this integrated signal by an automatically biased clipper. The videopart of the signal helps to build up a vertical sync pulse when heavy negative-going reflections (mountains) distort the video signal. The in/out sync-detector considers a signal out-of-sync when fifteen or more successive incoming vertical sync pulses are not in phase with a reference signal from the 625 divider. Therefore a distorted vertical sync signal needs only one out-of-fifteen pulses to be in phase to keep the system in sync. When the sixteenth successive out-of-sync pulse is detected, the direct/indirect sync switch is activated to feed the vertical sync signal directly out of the block at pin 2 (direct sync vertical output).
At the same time the 625 divider is reset by one of the sync pulses. After the reset pulse, if the 7th sliced vertical sync pulse coincides with a 625 divider window, the sync output pulse is presented again by the divider system and switch-over to indirect mode occurs.
In the direct mode, every 7th non-coinciding sliced vertical sync pulse will reset the counter. Thus a non-standard video signal will result in continuous reset pulses and the direct/indirect switch will remain in the direct position.

To avoid delay in vertical synchronization, caused by waiting time of the divider circuit after channel change or an unsynchronized camera change in the studio, information is fed from the horizontal coincidence detector to the automatic switch for the vertical sync pulse. The loss of horizontal synchronization sets the automatic switch to direct vertical sync. When horizontal coincidence is detected again the setting of the automatic switch depends on whether a standard video signal is received or not. When an external voltage between 2,5 V and 7,25 V is applied via pin 12 to the coincidence detector, the horizontal phase detector is switched to a short time constant and the automatic switch to direct vertical

FUNCTIONAL DESCRIPTION (continued)

sync. A voltage level on pin 12 > 8,25 V switches the horizontal phase detector to a short time constant, without affecting the indirect/direct vertical sync system which remains operational.

The video transmitter identification circuit detects when a sync pulse occurs during the internal gating pulse. This indicates the presence of a video transmitter and results in the capacitor connected to pin 10 being charged to 8 V. When no sync pulse is present the capacitor discharges to < 1 V. The voltage at pin 10 is compared with an internal d.c. voltage. The identification output at pin 9 is active when pin 10 is < 1,6 V (no video transmitter) and inactive (high impedance) when pin 10 is > 3,5 V. The vertical sync output pulse at pin 1 is inhibited when no video transmitter is identified, which prevents interference or noise affecting the frequency of the vertical output stage. This results in a vertical stable picture, plus vertical stable position information of tuning systems.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

Supply voltage				
horizontal (pin 14)	$V_{14\text{-}13}$	max.	13,2	V
vertical (pin 18)	$V_{18\text{-}13}$	max.	13,2	V
Total power dissipation	P_{tot}	max.	1020	mW
Storage temperature range	T_{stg}		−25 to +130	°C
Operating ambient temperature range	T_{amb}		−25 to +65	°C

CHARACTERISTICS

V_{14-13} = 12 V; V_{18-13} = 12 V; T_{amb} = 25 °C unless otherwise specified

parameter	symbol	min.	typ.	max.	unit
Supply (pins 14 and 18)					
Supply voltage range	$V_{14;18-13}$	10	12	13,2	V
Supply current (pin 14 + pin 18)	$I_{14} + I_{18}$	–	52	77	mA
Sync separator and noise gate (pin 2)					
Top sync level (note 1)	V_{2-13}	1	1,5	3,5	V
Sync pulse amplitude (peak-to-peak value) (note 2)	$V_{2-13(p-p)}$	0,07	–	1	V
Noise level	V_{2-13}	0,5	0,7	1,1	V
Slicing level (note 3)		35	50	65	%
Delay between sync input at pin 2 and phase detector output at pin 6*	t_d	–	0,40	–	μs
Phase detector (pin 6)					
Control voltage	V_{6-13}	0,5	2,8	5	V
Control sensitivity		–	1,2	–	V/μs
Phase locked loop					
Holding range (note 4)	Δf	–	± 1000	–	Hz
Catching range (note 4)	Δf	± 600	± 900	–	Hz
Control sensitivity		–	2000	–	Hz/μs
Phase modulation due to hum on the supply line (note 5)		–	2	–	μs/V

DEVELOPMENT SAMPLE DATA

* See waveforms Fig. 2.

CHARACTERISTICS (continued)

parameter	symbol	min.	typ.	max.	unit
Horizontal oscillator					
Output frequency					
free running	f_o	–	31,250	–	kHz
at pin 8	f_8	–	15,625	–	kHz
Temperature coefficient	T	–	$2{,}5 \times 10^{-4}$	–	K^{-1}
Frequency variation					
without tolerance of external components	Δf_o	–	–	4	%
when voltage at pin 14 drops to 6 V	Δf_o	–	–	10	%
when voltage at pin 14 increases from 10 to 13,2 V	Δf_o	–	–	0,5	%
Output pin 8					
voltage (no load; peak-to-peak value)	$V_{8\text{-}13(p\text{-}p)}$	10	–	–	V
current (peak-to-peak value)	$I_{8(p\text{-}p)}$	–	10	25	mA
Output resistance	$R_{8\text{-}13}$	–	433	–	Ω
Output pulse duty factor	δ	–	54	–	%
Delay between trailing edge of output pulse and end of sync pulse at pin 2	t_d	–	0,9	–	μs
Sandcastle pulse (pin 15)					
Output voltage (peak-to-peak value)	$V_{15\text{-}13(p\text{-}p)}$	9	–	–	V
Duration of upper part of output pulse*	t_p	3	3,6	4,4	μs
Duration of lower part of output pulse*	t_p	8,4	8,8	9,2	μs
Amplitude of lower part of output pulse (peak-to-peak value)*	$V_{15\text{-}13(p\text{-}p)}$	4	4,5	5	V
Output impedance	$\lvert Z_o \rvert$	–	200	–	Ω
Delay between trailing edge of sync pulse at pin 2 and leading edge of sandcastle pulse at pin 15*	t_d	–	0,9	–	μs

* See waveforms Fig. 2.

parameter	symbol	min.	typ.	max.	unit
Vertical sync pulse (pin 1)					
Output voltage (peak-to-peak value)	$V_{1\text{-}13(p\text{-}p)}$	10	–	–	V
Load resistor to pin 18	R_L	4	–	–	kΩ
Duration of output pulse during indirect synchronization	t_p	–	170	–	μs
Video transmitter identification circuit Pin 10					
Sync pulse present					
charge current	I_{10}	–	+ 100	–	μA
output voltage	$V_{10\text{-}13}$	–	8	–	V
No sync pulse					
discharge current	I_{10}	–	−100	–	μA
output voltage	$V_{10\text{-}13}$	–	–	1	V
Switching level output stage					
pin 9 active when:	$V_{10\text{-}13}$	1,6	1,9	2,5	V
pin 9 inactive when:	$V_{10\text{-}13}$	3,0	3,5	4,0	V
Pin 9 (note 6)					
Sync pulse present					
output current inactive	I_9	–	–	1	μA
No sync pulse					
output current active	I_9	2,5	4,0	5,0	mA
output voltage active (load ⩽ 0,1 mA)	$V_{9\text{-}13}$	10,5	11,0	–	V
Coincidence detector (pin 12)					
First switching level (note 7)					
voltage	$V_{12\text{-}13}$	1,7	2,0	2,2	V
required input current	I_{12}	0,8	–	–	mA
maximum allowed input current	I_{12}	–	–	1,5	mA
Second switching level* (note 8)					
voltage	$V_{12\text{-}13}$	7,25	7,75	8,25	V
required input current	I_{12}	–	2,2	3,0	mA
Voltage					
normal conditions	$V_{12\text{-}13}$	–	0,4	–	V
out-of-sync	$V_{12\text{-}13}$	–	2,5	–	V
during noise	$V_{12\text{-}13}$	–	1,0	–	V

* VDR conditions.

DEVELOPMENT SAMPLE DATA

Notes to characteristics

1. The video signal at pin 2 must have negative-going sync.
2. Up to 1 V peak-to-peak the slicing level is constant; at amplitudes exceeding 1 V peak-to-peak the slicing level will increase.
3. The slicing level is determined by the value of the resistor between pin 3 and pin 4. The 50% figure is obtained with a 5,6 kΩ resistor.
4. Values of external circuitry as shown in Fig. 1.
5. The voltage is a peak-to-peak value; the figure can be reduced to 0,6 μs/V (p-p) by connecting a 330 nF capacitor between pins 7 and 14.
6. The video transmitter identification output stage at pin 9 consists of a p-n-p current source with an n-p-n emitter-follower.
7. A voltage level between 2,5 V and 7,25 V switches the horizontal phase detector to a short time constant and the automatic switch to direct vertical sync.
8. A voltage level > 8,25 V switches the horizontal phase detector to a short time constant without affecting the operation of the automatic switch.

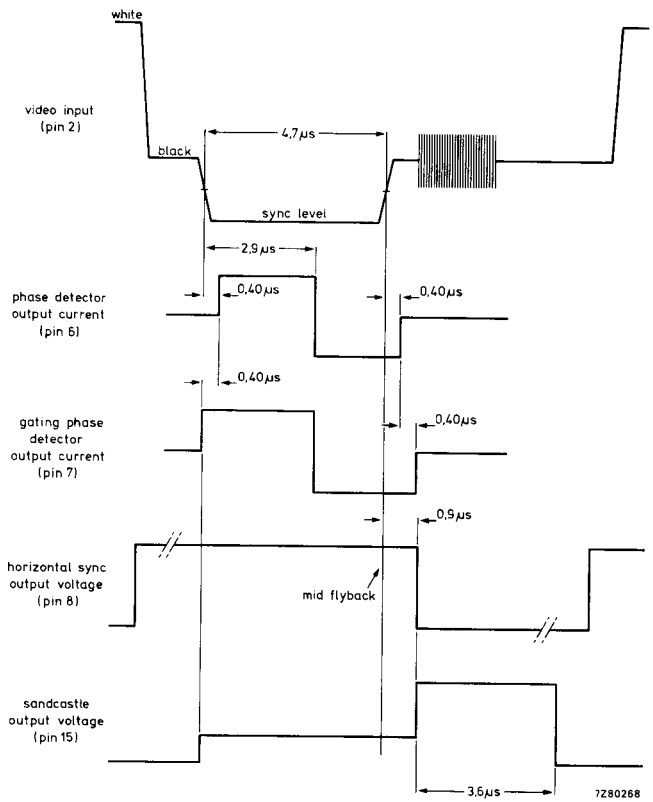

Fig. 2 Phase relationship between the input and output signals of the TDA3571B.

APPLICATION INFORMATION (see also Fig. 3)

The function is described against the corresponding pin number.

1. Vertical output pulse

A 10 kΩ resistor must be connected between pin 1 and the positive vertical supply line at pin 18. The pulse is obtained from the 625 divider circuit when standard input signals are received or from the sync separator when the signals are non-standard. The pulse is inhibited when no video transmitter is detected.

2. Video input

The video input signal must have negative-going sync pulses. The top-sync level can vary between 1 V and 3,5 V without affecting the sync separator operation. The slicing level is fixed at 50% for the sync pulse amplitude range 0,07 to 1 V which provides good sync separation down to pulses with an amplitude of 70 mV peak-to-peak. The slicing level is increased for sync pulses in excess of 1 V peak-to-peak. The noise gate is activated at an input level < 1 V, thus when noise gating is required the top sync level should be close to the minimum level of 1 V. When i.f. circuits with a noise gate are used (TDA2540; TDA2541) the noise gate of the TDA3571B is not required.

3. Sync separator slicing level output

The sync separator slicing level is determined on this pin. A slicing level of 50% is obtained by comparing this level with the black level of the video signal, which is detected at pin 4. The slicing level P is determined by the following formula:

$$P = \frac{R_S}{R_S + T_{hor}/T_{sync} \times 0{,}35\ k\Omega} \times 100\% = \frac{R_S}{R_S + 5{,}6\ k\Omega} \times 100\%$$

where R_S is the resistor (in kΩ) between pins 3 and 4. The capacitor that is connected to pin 3 must be between 0,47 μF and 4,7 μF.

4. Black level detector output

The black level of the input signal is detected on this pin. This is required to obtain good sync separator operation. A 47 μF capacitor in series with a resistor of 82 Ω must be connected to this pin. A 5,6 kΩ resistor connected between pin 3 and pin 4 results in a slicing level of 50%.

5. Vertical sync pulse integrator biasing network

The vertical sync pulse is obtained by integrating the composite sync signal in an internal RC-network. An external RC-network is required for the correct biasing of this circuit for various input conditions. Typical values are: R = 68 kΩ; C = 10 μF. The resistor influences the delay of the direct vertical sync pulse.

6. Horizontal phase detector output

The control voltage for the horizontal oscillator is obtained on this pin. The output current is about 2 mA.

7. Reference voltage horizontal frequency control stage

This pin has two functions. It is used to decouple the reference voltage for the frequency control of the horizontal (so a good suppression of interference is obtained which may be present on the supply line). It also controls the reference waveform for symmetrical gating of the horizontal synchronization, thus providing good noise immunity.

APPLICATION INFORMATION (continued)

8. Horizontal sync pulse output

This pulse is obtained from the horizontal oscillator via a divider circuit. The duty factor is 54%. The trailing edge of this pulse occurs 0,9 μs after the end of the video sync pulse input at pin 2. Because of this phase relationship the horizontal sync pulse can drive directly the TDA2581.

9. Video transmitter identification output

This is an emitter-follower output which will be inactive (high-impedance) when the level at pin 10 is $>$3,5 V (video transmitter detected). The output will be active high when the level at pin 10 is $<$ 1,6 V (no video transmitter detected). This feature can be used for search-tuning and sound-muting.

10. Video transmitter identification

A 47 nF capacitor must be connected to this pin. It charges to a level of 8 V when a sync pulse is detected, and discharges to a level of $<$ 1 V when no sync pulse is detected.

11. Gating switch

This pin is used to switch the time constant of the flywheel filter. The pin condition is determined by the coincidence detector (pin 12). During in-sync or when only noise is being received pin 11 assumes ground level, which results in a long time constant and good noise immunity.

12. Coincidence detector output

A 1 μF capacitor must be connected to this pin. The output voltage depends on the oscillator condition (synchronized or not) and on the video input signal. There are two switching levels at pin 12. At the first switching level when the output voltage is $<$ 1,85 V, the flywheel filter is switched to a long time constant and the gating of the phase detector is switched on. When the output voltage is $>$ 1,85 V, the flywheel filter has a short time constant, and the gating of the phase detector is switched off. The result is that during noise the flywheel filter time constant remains long thus preventing large shifts in the frequency of the horizontal oscillator (and screening of the horizontal output transformer). At the second switching level when the output voltage is $>$ 8,25 V the sync system is switched to a short time constant while the indirect/direct vertical sync system remains fully operational. This condition is suitable for VCR application.

13. Negative supply (ground)

14. Positive supply horizontal oscillator

Interference and hum on this supply line can affect the oscillator frequency. It is therefore necessary to have separate decoupling of this pin with respect to pin 18.

15. Sandcastle pulse output

This pulse is composed of two parts. The lower part has an amplitude of typ. 4,5 V peak-to-peak and a width of max. 9,2 μs (for phase relationship see Fig. 2). The upper part has a total amplitude in excess of 9 V peak-to-peak and a width of max. 4,4 μs. The leading edge of this pulse has a delay of 0,9 μs with respect to the trailing edge of the sync pulse at the input (pin 2). This pulse can directly drive the burst gate/black level clamp input of the TDA2560.

16. RC-network horizontal oscillator

Stable components should be chosen for good frequency stability. For adjusting the frequency a part of the total resistance must be variable. This part must be as small as possible, because of poor stability of variable carbon resistors.
The oscillator can be adjusted when pins 7 and 17 are short circuited (see Fig. 3).

17. Horizontal oscillator control pin

18. Positive supply sync separator and divider circuit (vertical)

This supply requires only simple decoupling. The typical combined current draw of pins 14 and 18 is 52 mA.

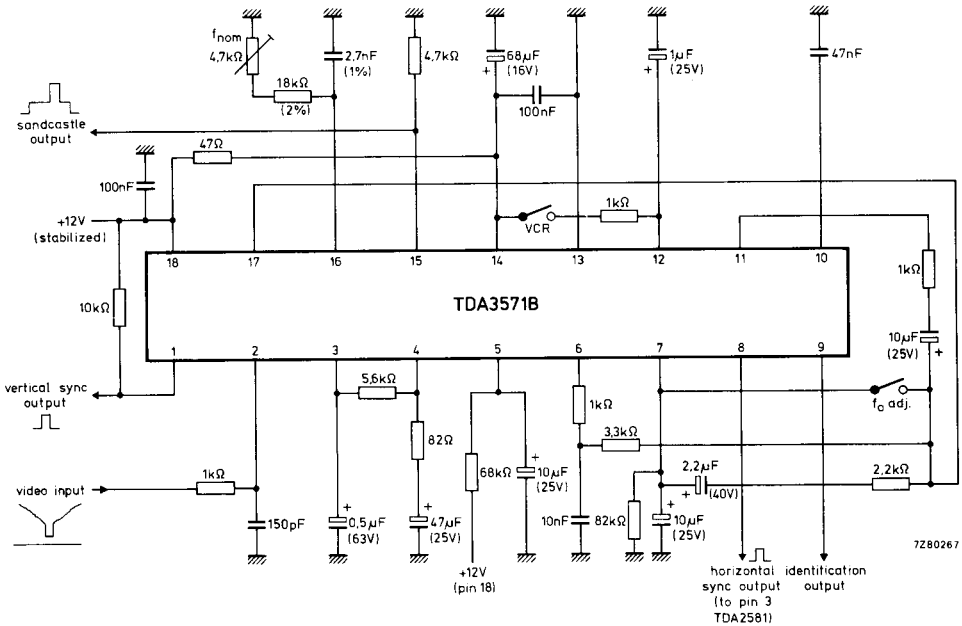

Fig. 3 Typical application circuit diagram; for combination of the TDA3571B with the TDA2581.

DEVELOPMENT SAMPLE DATA